Characteristic description

TM1680 is a driver chip for memory exchange LED display control, which can select multiple ROW/COM modes (32ROW/8COM and 24ROW/16COM), and can be used to drive dot matrix LEDs. The chip provides 16 levels of pulse width modulation control output set by software, which can adjust the brightness of LED cycle display. Using the serial interface (I2C communication interface) serial input method, you can easily enter the command mode (COMMAND, MDOE) and data mode (DATA, MODE), and only need simple commands to establish the main control chip and TM1680. communication. Continuous output display can be performed through TM1680, which has wide application in the display of LED lights, such as industrial instrument control, digital clock/thermometer/counter/voltmeter display, instrument data readout, LED display, smart bracelet and other applications. This product has excellent performance and reliable quality.

Features

- Working voltage 2.4～5.5V
- 32ROW*8COM and 24ROW*16COM are optional
- Comprehensive display memory - 64*4 display RAM (32ROW*8COM), 96*4 display RAM (24ROW*16COM)
- 16 levels PWM control brightness
- Built-in 256KHz RC oscillator
- I2C interface (SDA, SCL) communication
- Data Mode and Command Mode Instructions
- Selectable NMOS output channel and PMOS output channel
- Package form: LQFP48, LQFP52

Internal Structure Diagram

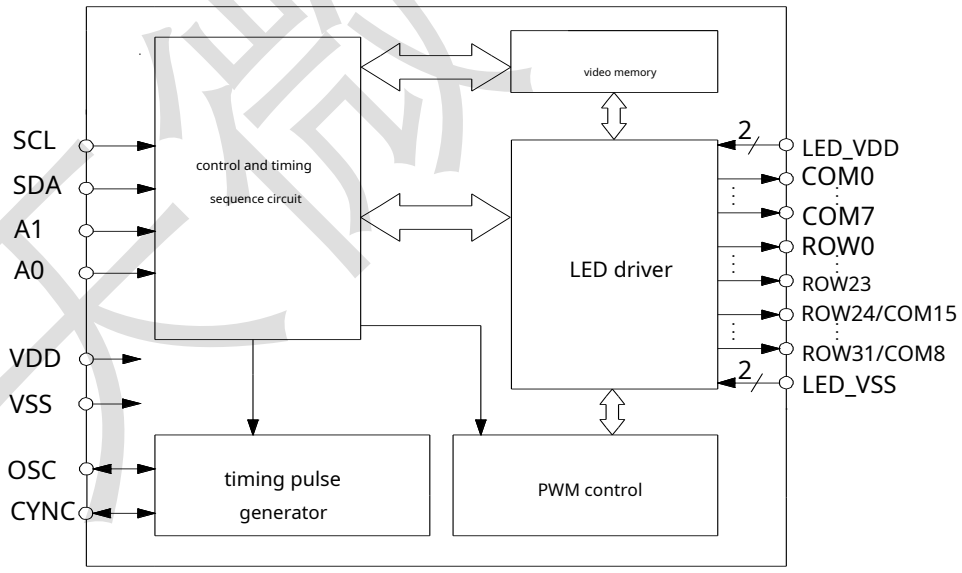


figure 1

Pin arrangement

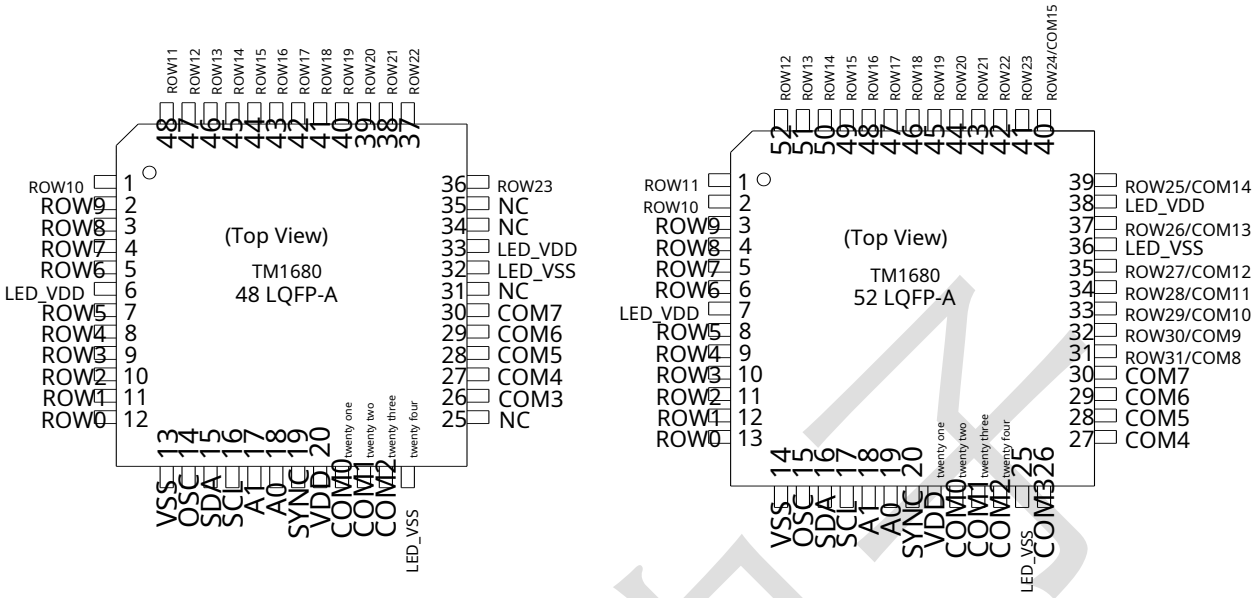


figure 2

pin function

Pin name	Pin number	I/O	Function Description
VDD	twenty one	-	Positive pole of chip logic power supply
VSS	14	-	Negative pole of chip logic power supply
LED_VDD	7/38	-	The positive pole of the LED drive power supply must be connected to the same voltage as the 21 pin VDD
LED_VSS	25/36	-	Negative pole of LED drive power supply, connected to VSS
ROW0～ROW23	1～6/8～13/41～52	O	LED row driver output
ROW24/COM15 ~ROW31/COM8	31～35/37/39/40	O	LED row driver output or common input
COM0～COM7	22～24/26～30	O	LED common input
SYNC	20	I/O	If the main trigger mode or external extended trigger mode is selected, the synchronization signal will be output from the SYNC pin; if the passive mode is selected, the synchronization signal will be input from the SYNC pin.
OSC	15	I/O	When the RC oscillator main trigger mode is selected, the system clock is generated by the on-chip RC oscillator and output from the OSC pin; if the passive mode or external extended trigger mode is selected, the system clock is input from the OSC pin externally.
A0	19	I	Slave address extension bit, built-in pull-up resistor.
A1	18	I	Slave address extension bit, built-in pull-up resistor.
SCL	17	I	I2C communication clock input. When the SCL signal rises, the data on the SDA line is written into the TM1680, which has a built-in pull-up resistor.
SDA	16	I/O	I2C communication data input/output port, external pull-up resistor is required for application.

* Remarks: The pin numbers in the above table take the LQFP52 package as an example. Different packages have different pin positions, please refer to pins for details Pareto. The display mode of 48PIN package is only 24*8.

Input and output equivalent circuit

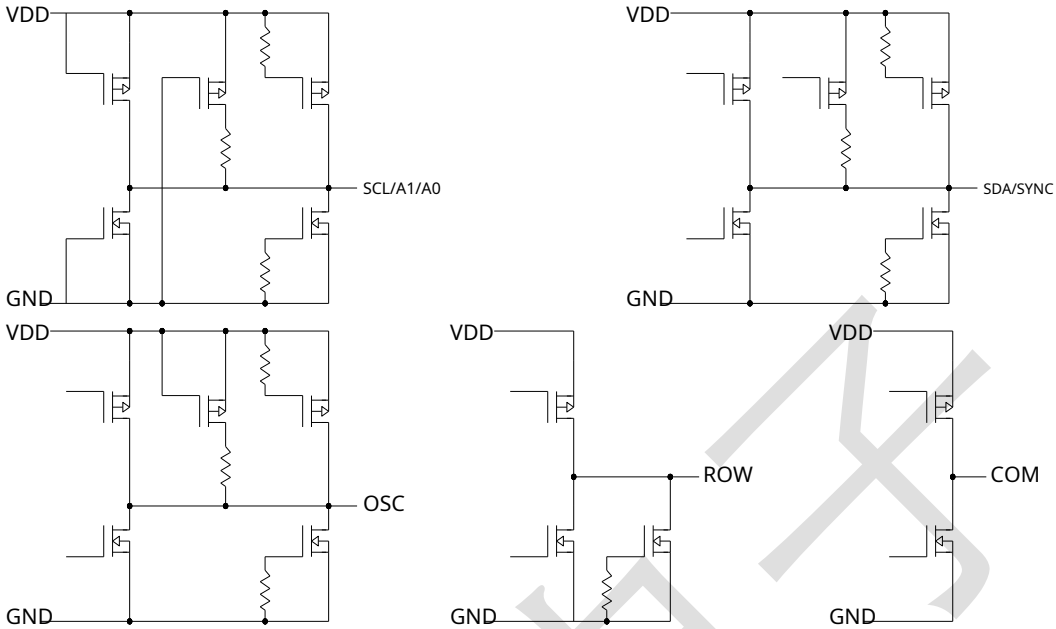


image 3

The integrated circuit is an electrostatic sensitive device. It is easy to generate a large amount of static electricity when used in a dry season or in a dry environment. Electrostatic discharge may damage the integrated circuit. Tianwei Electronics recommends that all appropriate preventive measures be taken for the integrated circuit. Improper operation and welding may cause damage to the integrated circuit. ESD damage or performance degradation, the chip does not work properly.

Limit parameter (1) (2)

parameter name	parameter symbol	limit value	one bit
Logic supply voltage	VDD	VSS-0.3V ～ VSS+6V	V
Input voltage range SDA,SCL,OSC,SYNC	Vin	VSS-0.3～VDD+0.3	V
range of working temperature	top	- 40～+85	℃
storage temperature range	Tstg	- 55～+125	℃

(1) The chip works under the above limit parameters for a long time, which may cause the reliability of the device to be reduced or permanently damaged. Tianwei Electronics does not recommend any parameter to reach or exceed these limit values in actual use.

(2) All voltage values are tested relative to system ground.

Recommended working conditions

parameter name	parameter symbol	minimum value	typical value	maximum value	
Operating Voltage	VDD	2.4	5.0	5.5	V
Input low level voltage	Vil	0	-	0.3VDD	V
Input high level voltage	Vih	0.7VDD	-	5	V

DC electrical characteristics

Tested at VDD=2.4~5.5V and Ta=+25℃, unless otherwise specified				TM1680			unit
parameter name	parameter symbol	VDD	Test Conditions	minimum value	typical value	maximum value	
Working current	IDD	5.0V	On-chip RC, no load, open display		0.3	0.6	mA
stand-by current	ISTB	5.0V	Power saving mode, no load		0.1	10	μA
OSC,SYNC,SDA sink current	IOL1	5.0V	Vol=0.5V	18	25	-	mA
OSC,SYNC,SDA source current	IOH1	5.0V	Voh=4.5V	- 10	- 13	-	mA
ROW sink current	IOL2	5.0V	Vol=0.5V	12	16	-	mA
ROW source current	IOH2	5.0V	Voh=4.5V	- 50	- 70	-	mA
COM sink current	IOL3	5.0V	Vol=0.5V	250	350	-	mA
COM source current	IOH3	5.0V	Voh=4.5V	- 45	- 60	-	mA
Pull-up resistor	Rph	5.0V	SDA,SCL,OSC,SYNC	18	27	40	kΩ

Switching characteristics

Operating temperature is tested at 25°C unless otherwise stated			VDD=2.4V~5.5V		VDD=3.0V~5.5V		unit
parameter name	parameter symbol	Test Conditions	the smallest	maximum	the smallest	maximum	
Clock frequency	f	Chip internal clock	-	100	-	400	kHZ
bus idle time	tBUF	bus at next time the space before the bell free time	4.7	-	1.3	-	μs
Start signal hold time	tHD:STA	-	4	-	0.6	-	μs
SCL low time	tLOW	-	4.7	-	1.3	-	μs
SCL high level time	tHIGH	-	4	-	0.6	-	μs
Start signal setup time	tSU:STA	-	4.7	-	0.6	-	μs
data hold time	tHD:DAT	-	0	-	0	-	μs
data creation time	tSU:DAT	-	250	-	100	-	ns
SDA/SCL rise time	tr	-	-	1	-	0.3	μs
SDA/SCL fall time	tf	-	-	0.3	-	0.3	μs
Stop signal setup time	tSU:STO	-	4	-	0.6	-	μs
Noise cancellation on SDA/SCL input time	wxya	Noise cancellation time	-	20	-	20	ns

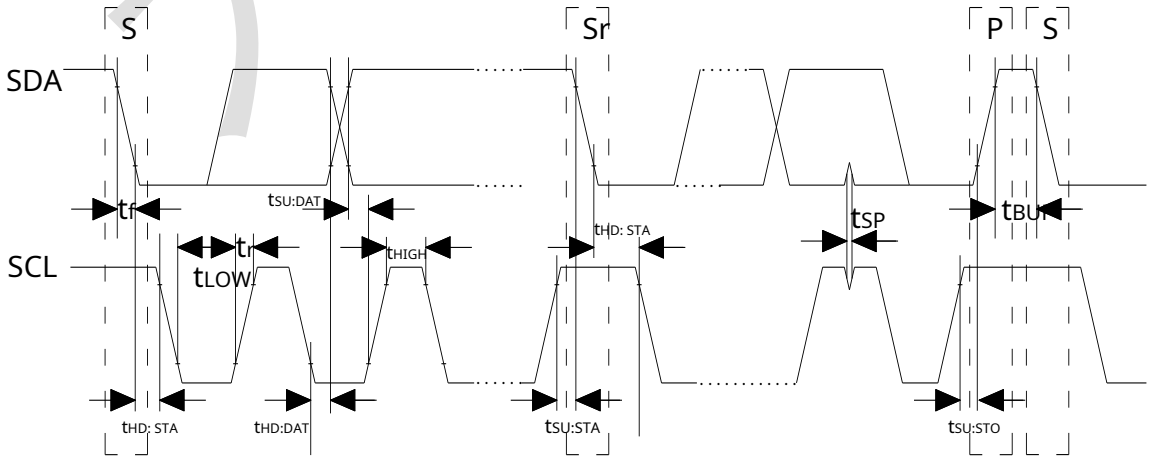
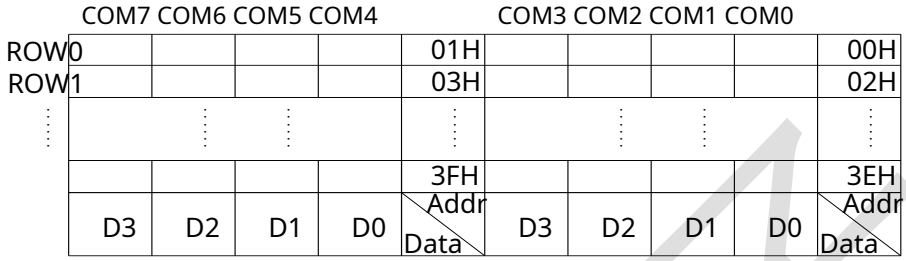


Figure 4

Functional description

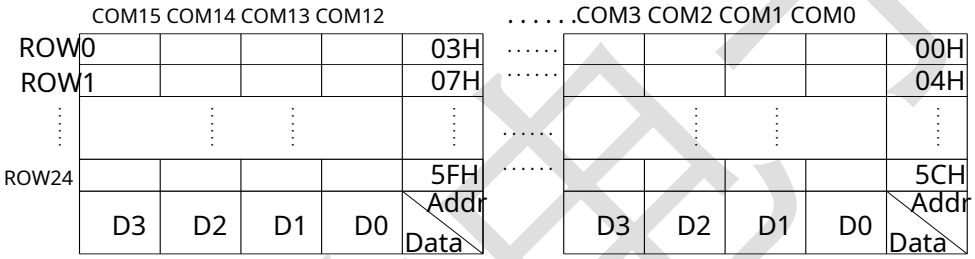
1 Display memory (RAM)

The static display memory contains two formats of 64*4 bits and 96*4 bits to store the data to be displayed. If the mode 32ROW/8COM is selected, the storage space of RAM is 64*4 bits; if the mode 24ROW/16COM is selected, the storage space of RAM is 96*4 bits. The data in RAM is directly mapped to the LED display driver, if the data in RAM is set to "1", the corresponding LED will be lit. Figure 5 and Figure 6 below show the mapping from RAM to LED:



32 ROW & 8 COM for 64×4 Display RAM

Figure 5



24 ROW & 16 COM for 96×4 Display RAM

Figure 6

2 system clock

The system clock of TM1680 is used to generate the clock frequency of system work. The LED drive clock and system clock can be taken from the on-chip RC oscillator (256KHz) or input from an external clock using S/W settings. The structure of the system oscillator is shown in Figure 7. When the SYS DIS command is executed, the system clock stops and the LED duty cycle will be turned off (this command is only applicable to the on-chip RC oscillator). Once the system clock is stopped, the LEDs will go blank and the time base will lose its functionality. The LED_OFF command is used to turn off the LED duty cycle. After the LED duty cycle is turned off, use the SYS DIS command to save power consumption and act as a power saving command; if the off-chip clock source is selected, use the SYS DIS command to disable the oscillator and execute power saving mode. The crystal oscillator can provide the clock frequency through the OSC pin, in this case, the system will not be able to enter the power saving mode. When the system is powered on, TM1680 is in SYS DIS state by default.

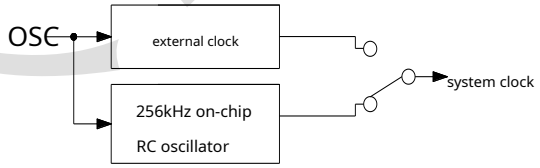


Figure 7

3 LED driver

TM1680 contains 256 (32*8) and 384 (24*16) LED drivers in two modes, which can be set to 32*8 or 24*16 display mode, and N-MOS or P-MOS output can be selected through the COM port output channel. These features make TM1680 suitable for different LED applications. The LED driving clock comes from the system clock, and the driving clock generally chooses the on-chip RC oscillator 256KHz or an extended external oscillator. For detailed setting commands, see the command overview table.

4 cascade operation

In cascade operation, the first cascaded chip is set to master mode, and its pins SYNC and OSC are used as outputs; the second cascaded chip is set to slave mode, and its pins SYNC and OSC are used as inputs , and connect with the SYNC and OSC pins of the host chip. The device address of TM1680 includes 2 external address selection bits A1 and A0, so up to 4 TM1680 can be connected to the same bus. Please refer to the cascade application circuit diagram for detailed settings. A1\A0 has a built-in pull-up resistor. When driving the chip alone, A1\A0 can be suspended. At this time, the slave address of TM1680 is 0xe7.

5 LED drive mode output waveform

The output waveform of 32×8 N-MOS open-drain output drive mode is shown in the figure below (Tclk=1/Fsys):

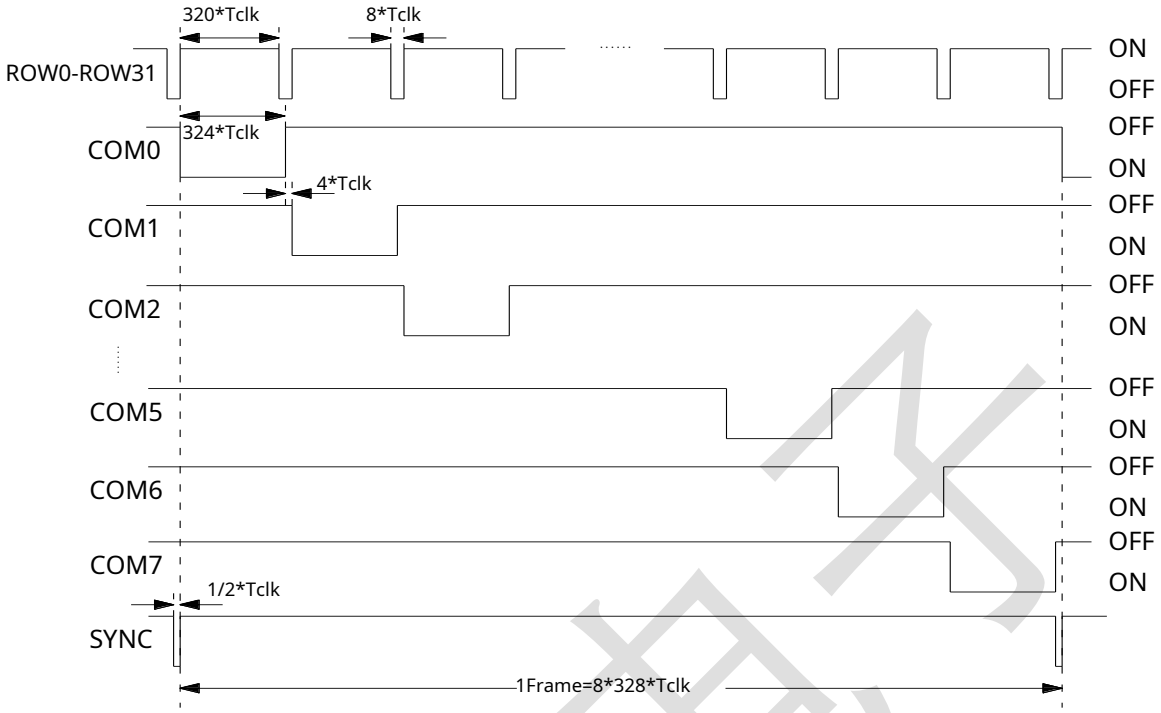


Figure 9

24×16 P-MOS open-drain output drive mode (Tclk=1/Fsys, COM pin plus transistor):

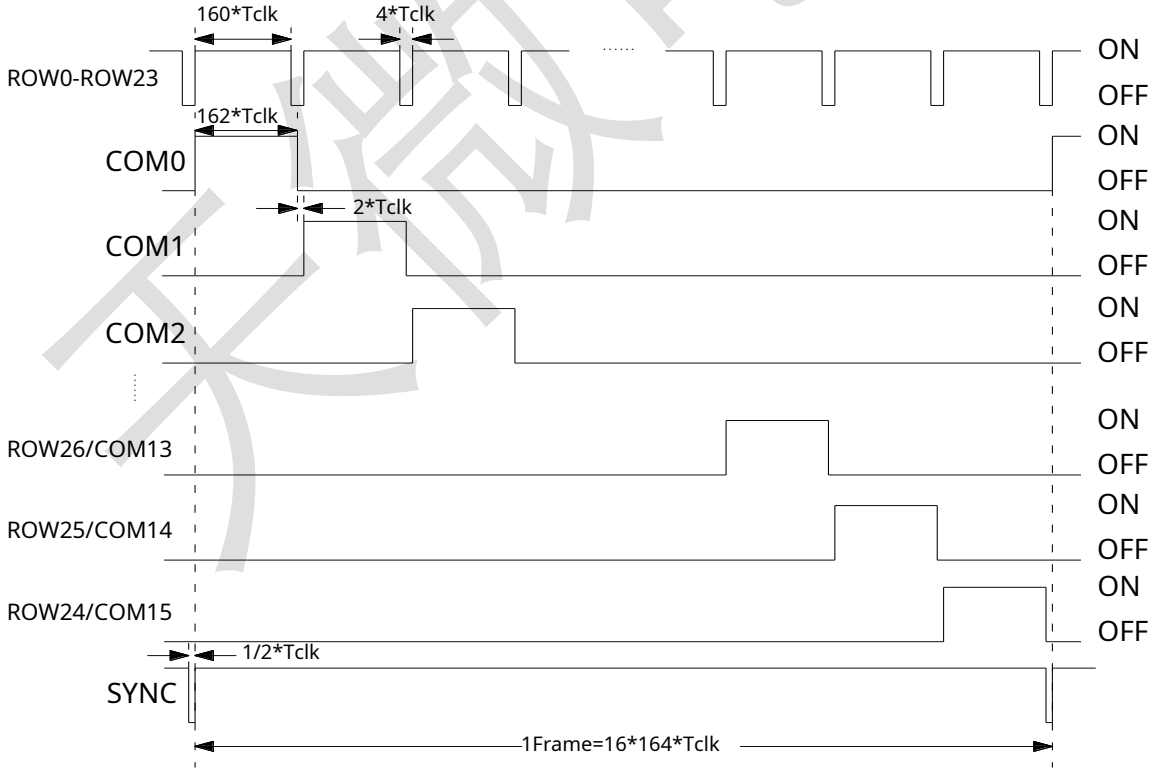


Figure 10

6 flash

TM1680 has a blinking function, which can make all LEDs blink at a certain frequency. The blinking rate can be set by the Blink command, which can be divided into 2Hz/1Hz/0.5Hz. The following is the output waveform with a flicker frequency of 2Hz:

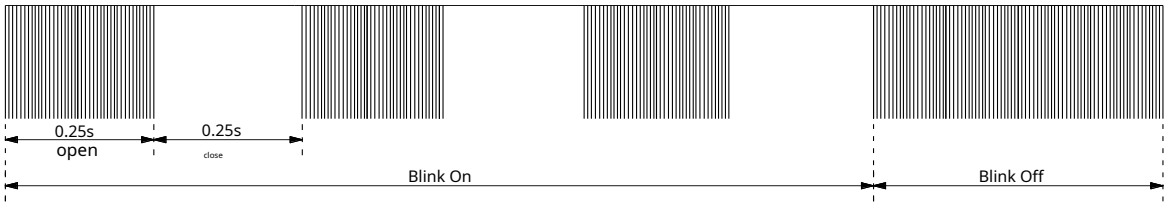


Figure 8

7 Brightness adjustment settings

TM1680 can perform multiple brightness controls by setting the PWM drive pulse width at the ROW terminal. Figure 11 below shows the output waveforms of the COM and ROW terminals under different duty ratio conditions: (1) T=20×Tclk (32×8 drive mode); (2) T=10×Tclk (24×16 drive mode); (3)Tclk=1/Fsys

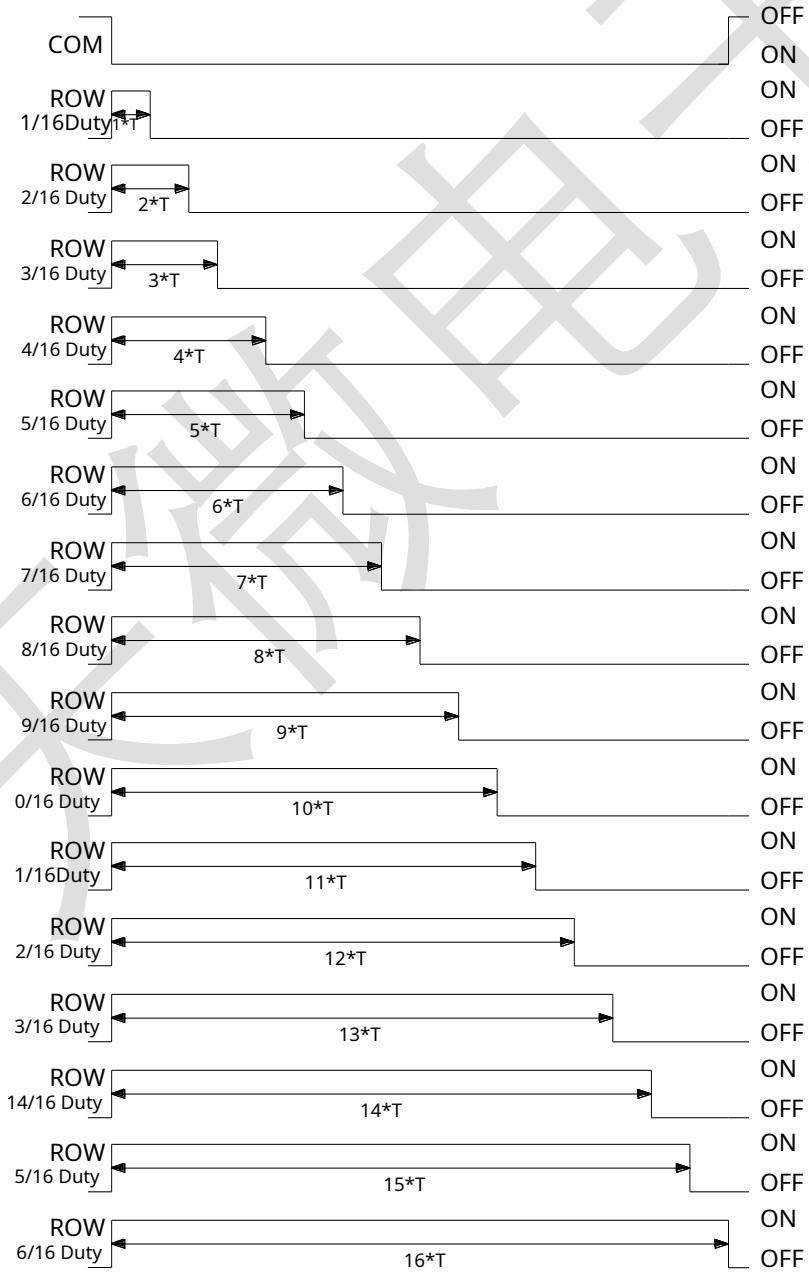


Figure 11

8 command format

When the chip is inputting commands or displaying data, the following steps must be followed: (1)

Form a start condition

(2) Send the slave address (Slave Address) (3)

Command, display data transmission

(4) Form a stop condition

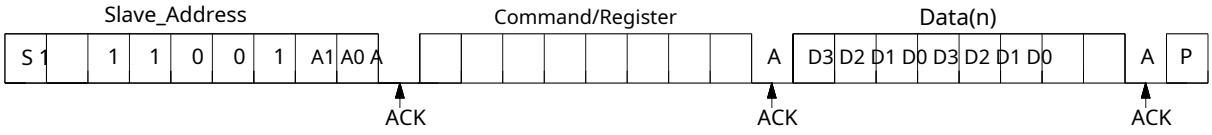


Figure 12

9 I2C serial interface

The chip uses the I2C protocol 2-wire serial interface for data transmission, including a serial data line SDA and a clock line SCL, the two lines have built-in pull-up resistors, and the bus is high when the bus is idle.

The controller generates a start signal every time data is transmitted, and uses synchronous serial to transmit data, and TM1680 responds with an ACK response signal after receiving a byte of data. Each byte sent on the SDA line must be 8 bits, and there is no limit to the number of bytes that can be sent per transfer. Each byte must be followed by an ACK response signal. When the ACK signal is not needed, a low level "L" needs to be input from the 8th signal falling edge to the 9th signal falling edge of the SCL signal. When the data is transmitted from the highest bit, the controller generates a stop signal to terminate the bus transmission, and resends the start signal during data transmission without the stop signal.

When SCL is high, the data on SDA remains stable; SDA is allowed to change when SCL is low. If SCL is at a high level, a falling edge occurs on SDA, which is considered a start signal; if SCL is at a high level, a rising edge generated on SDA is considered a stop signal. As shown below:

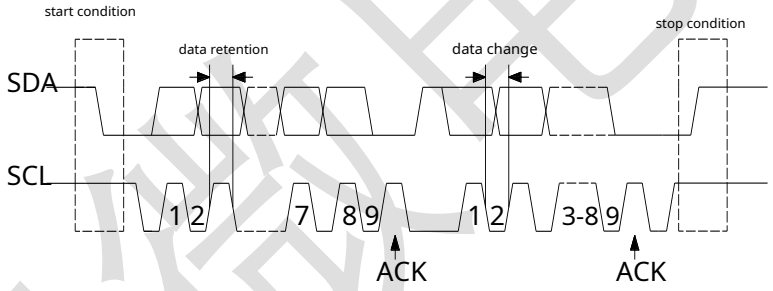


Figure 13

Timing diagram

1 Write command operation

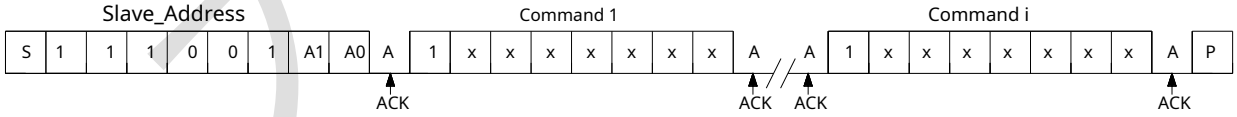


Figure 14

As shown in Figure 15, the upper 6 bits of the 8-bit slave address byte of the slave device are fixed at 111001, and the next 2 bits A1 and A0 are external address bits of the device.

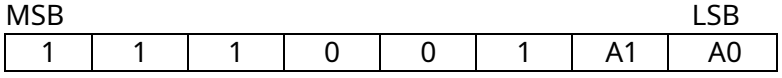


Figure 15

2 byte write operation

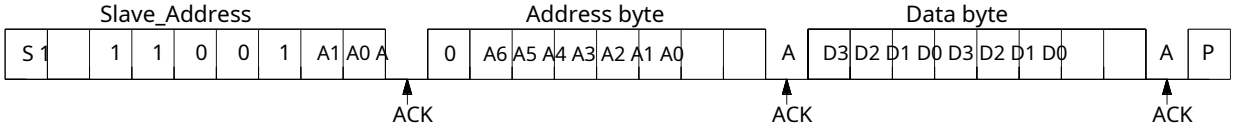


Figure 16

3 page write operations

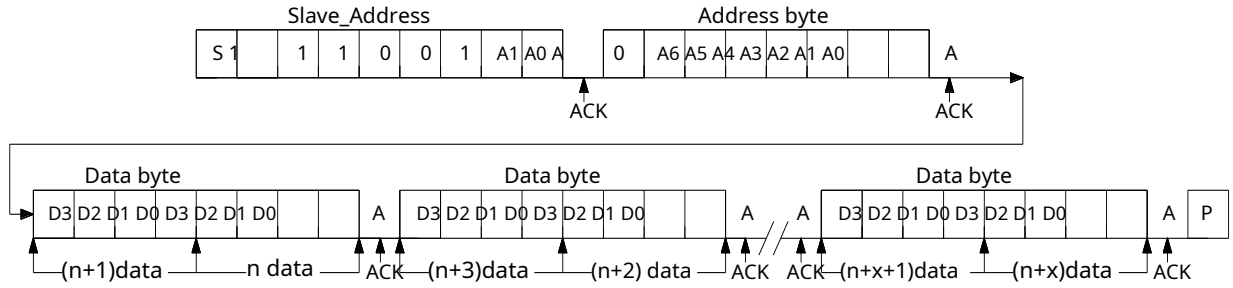


Figure 17

4 Write command + write data operation

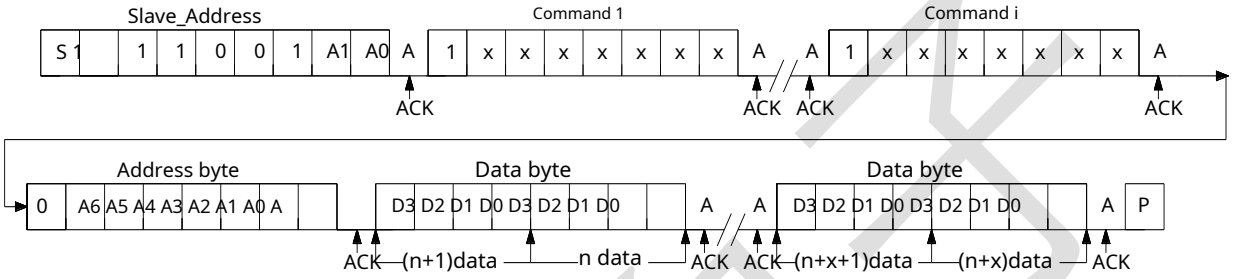


Figure 18

application circuit

Low-power LED application (direct drive mode): 32ROW*8COM mode example diagram19

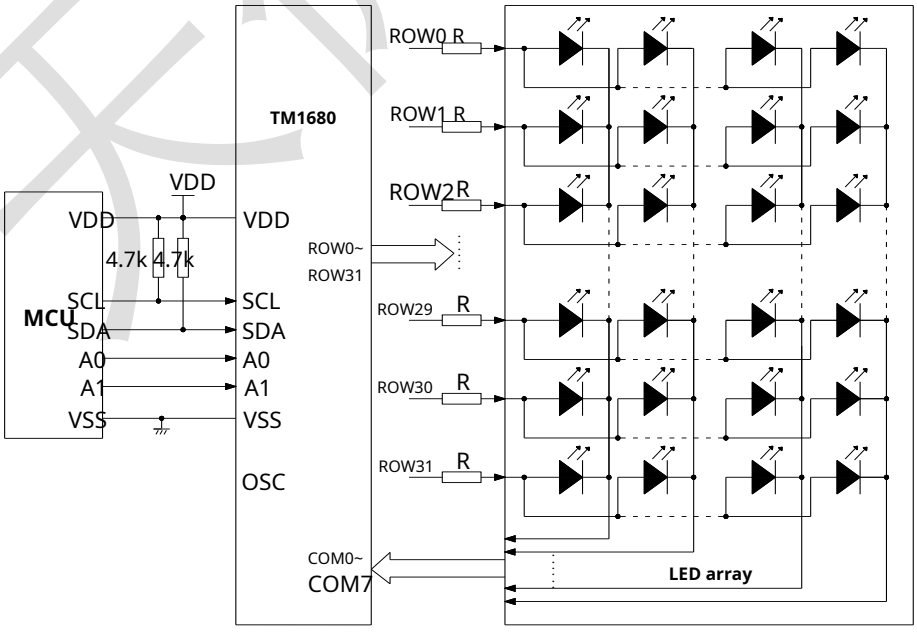


Figure 19

Low-power LED application (direct drive mode): 24ROW*16COM mode example diagram20

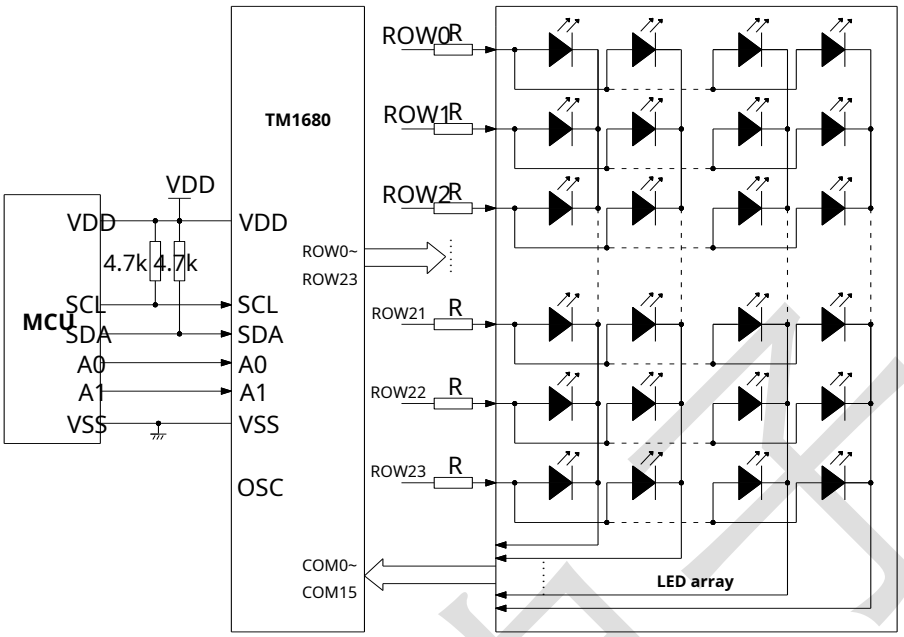


Figure 20

Medium power consumption LED application (COM plus transistor driving mode): 32ROW*8COM mode example diagramtwenty one

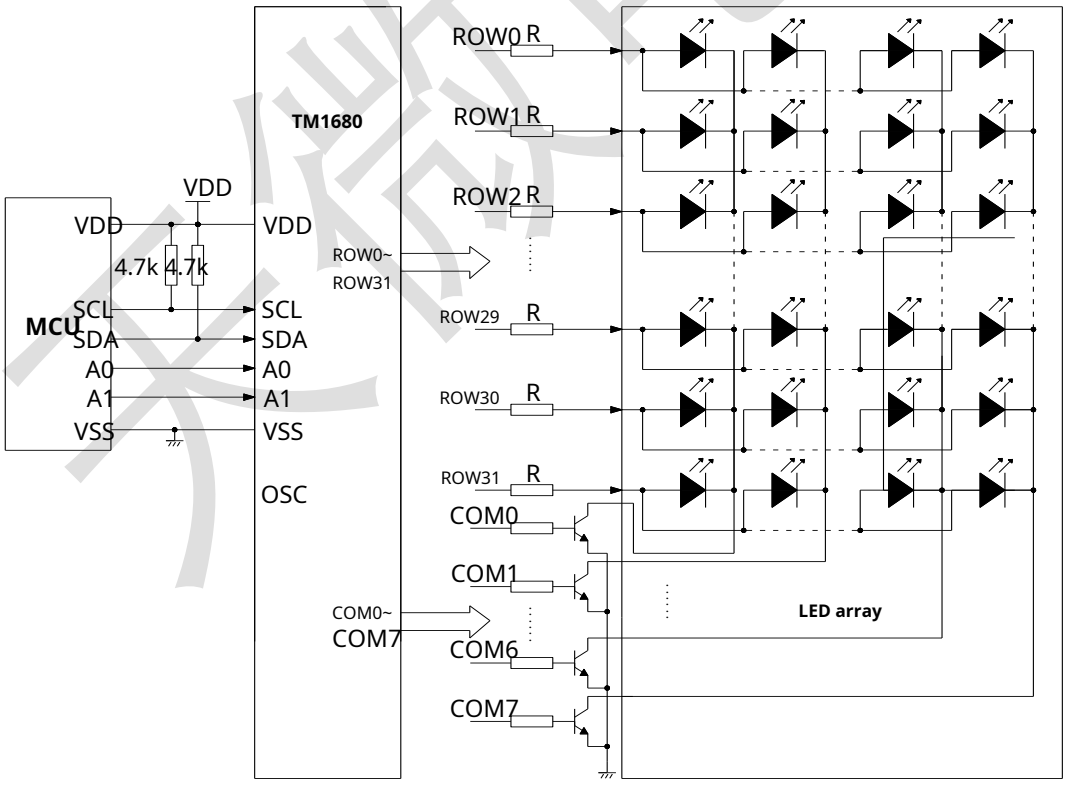


Figure 21

Medium power consumption LED application (COM plus transistor driving mode): 24ROW*16COM mode example diagramtwenty two

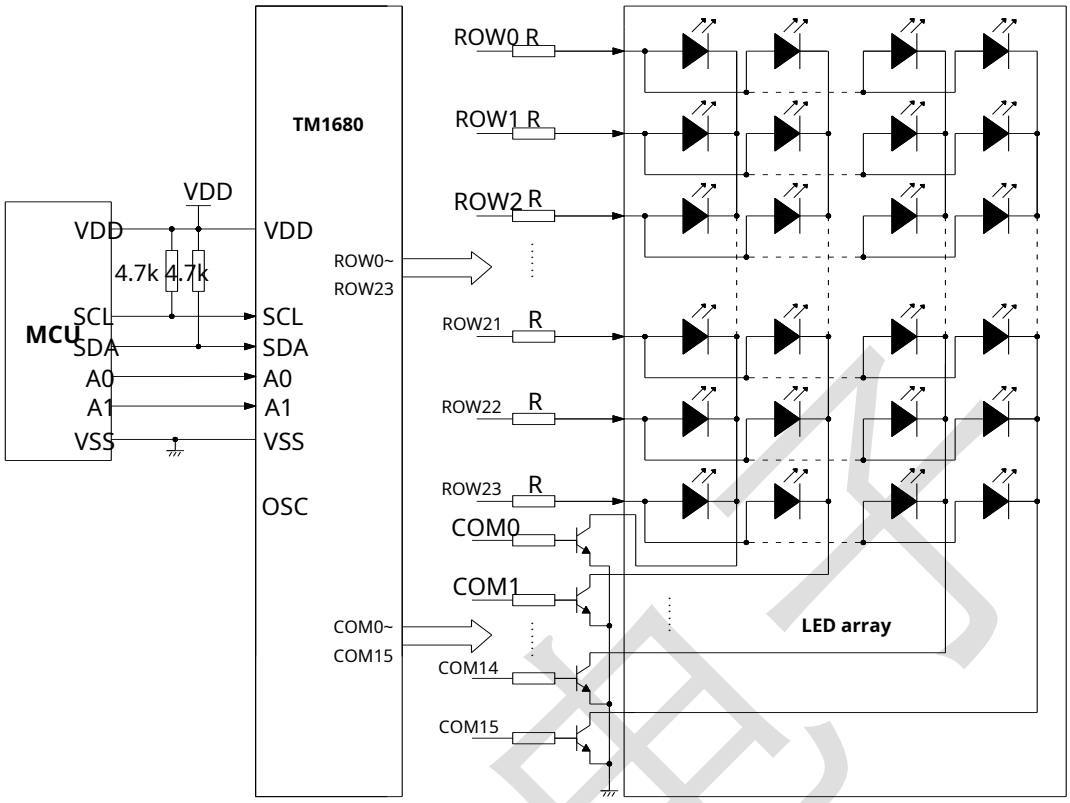


Figure 22

High-power LED application (ROW and COM plus transistor drive mode): 32ROW*8COM mode example diagramtwenty three

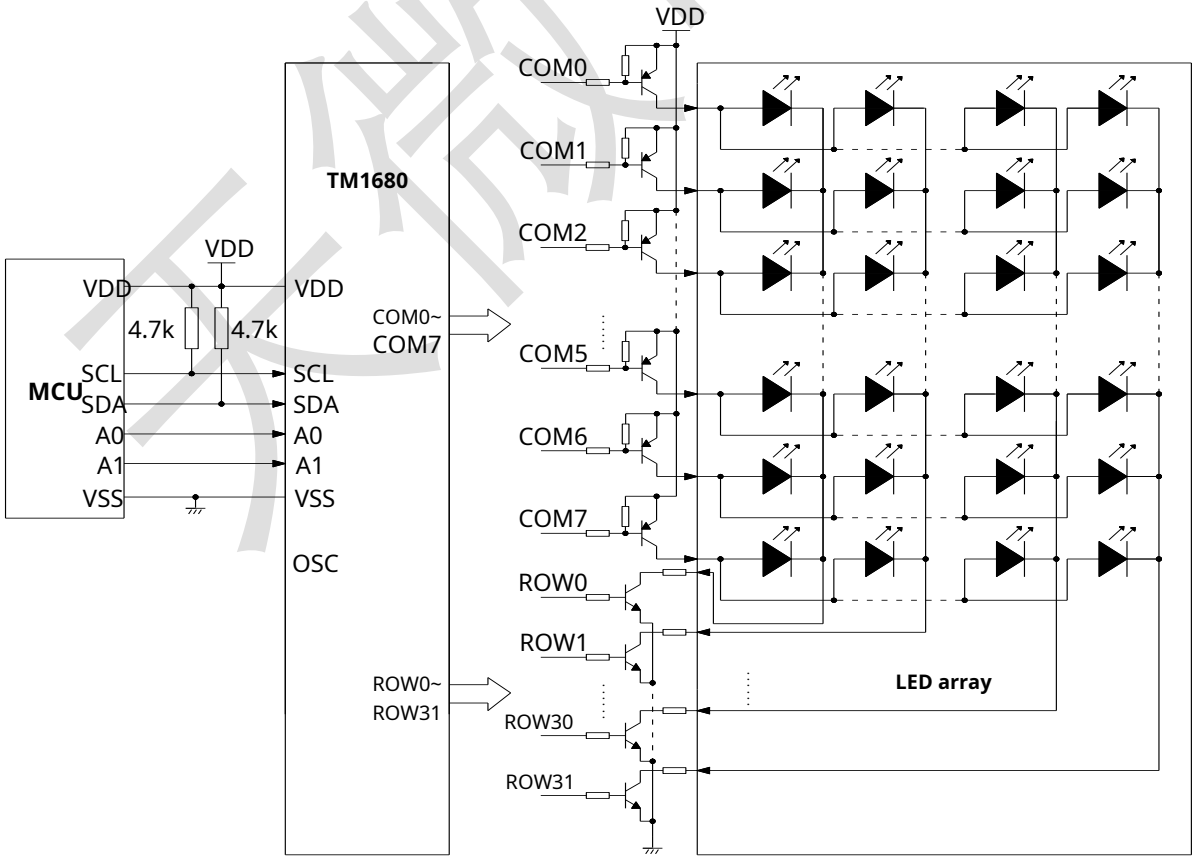


Figure 23

High power consumption LED application (ROW and COM plus transistor driving mode): 24ROW*16COM mode example diagramtwenty four

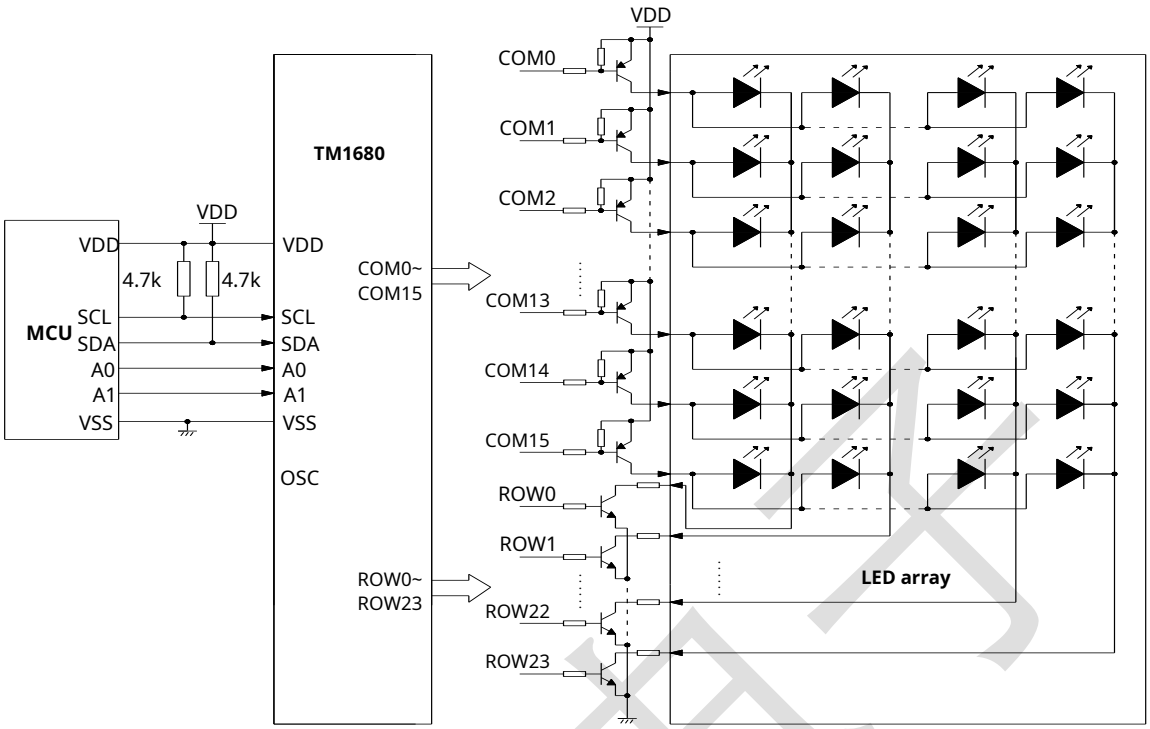


Figure 24

Cascade application (direct drive mode): 32ROW*8COM mode example diagram25

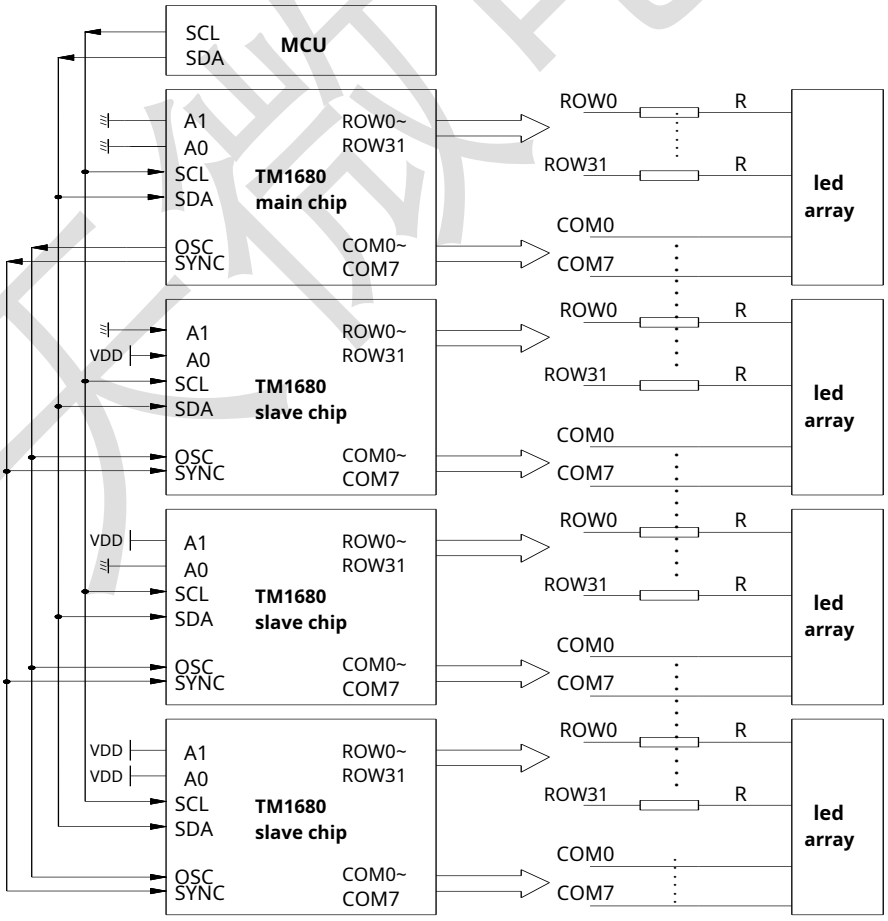


Figure 25

Cascade application (COM plus transistor drive mode): 32ROW*8COM mode example diagram26

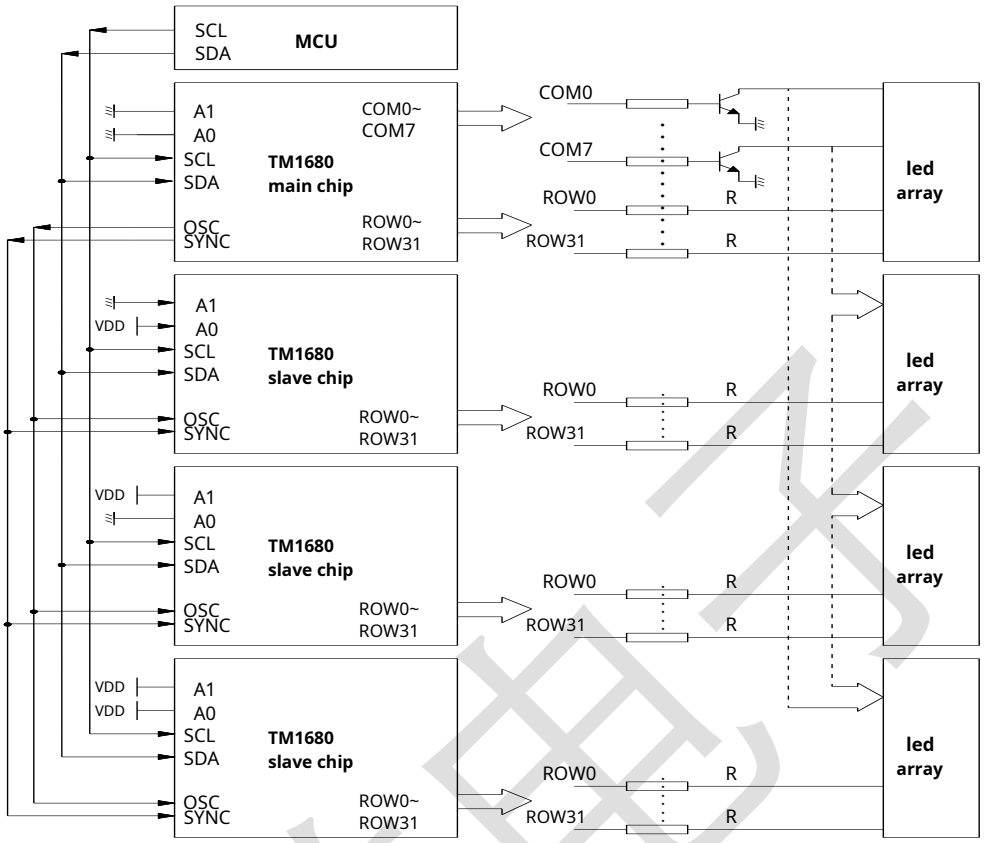


Figure 26

Cascade application (direct drive mode): 24ROW*16COM mode example diagram27

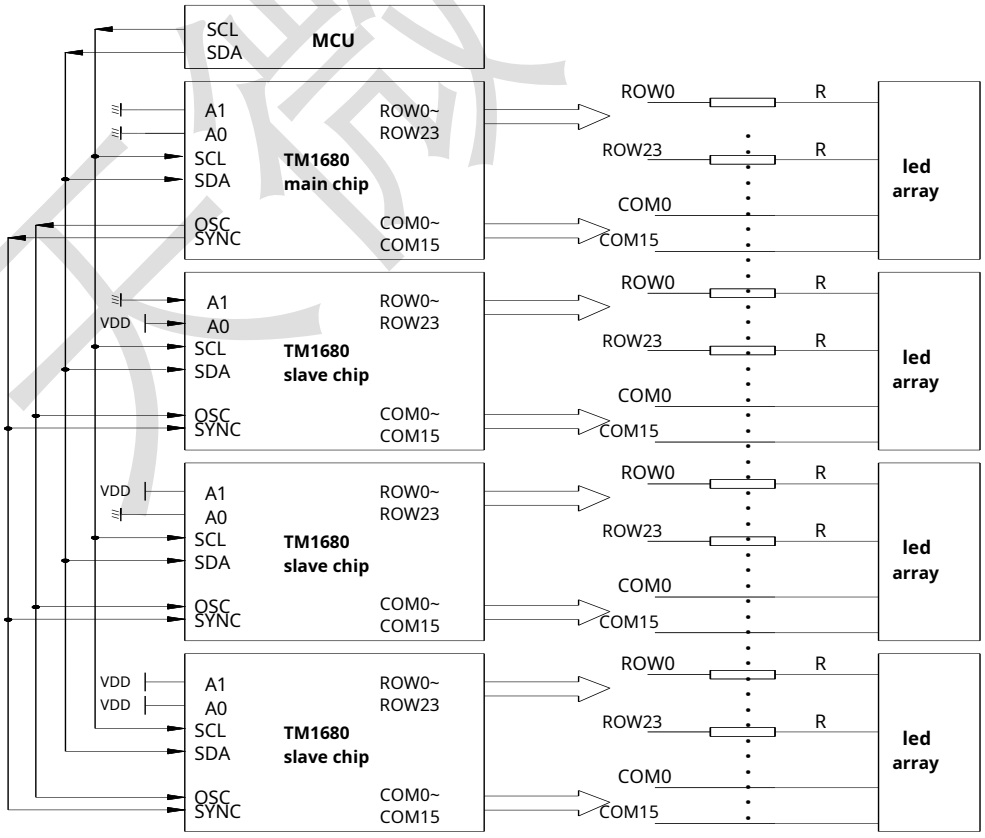


Figure 27

Cascade application (COM plus transistor drive mode): 24ROW*16COM mode example diagram28

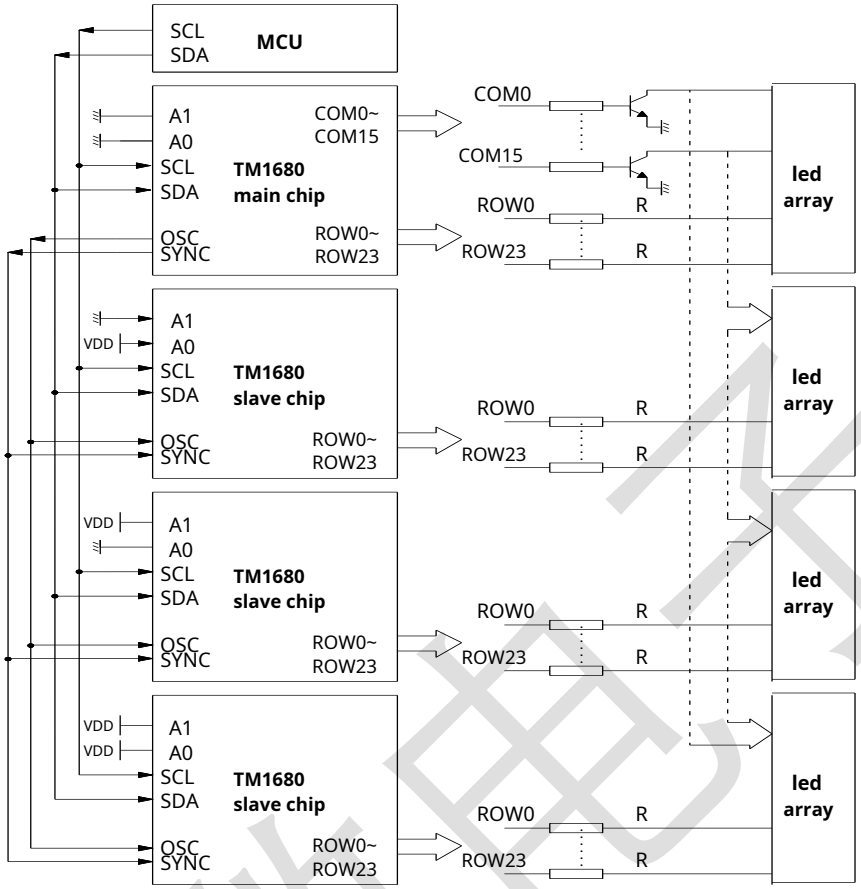
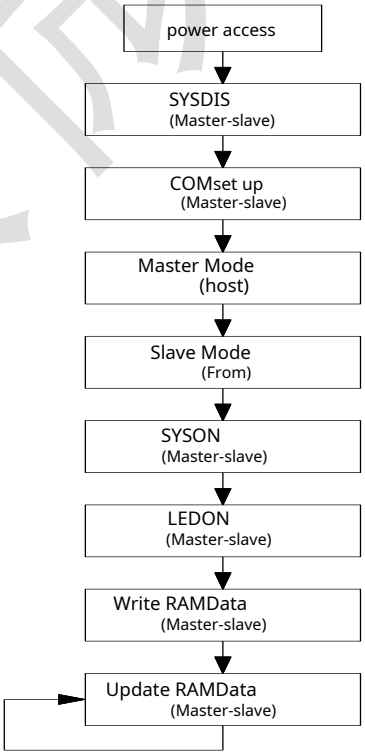


Figure 28

General Design Flowchart



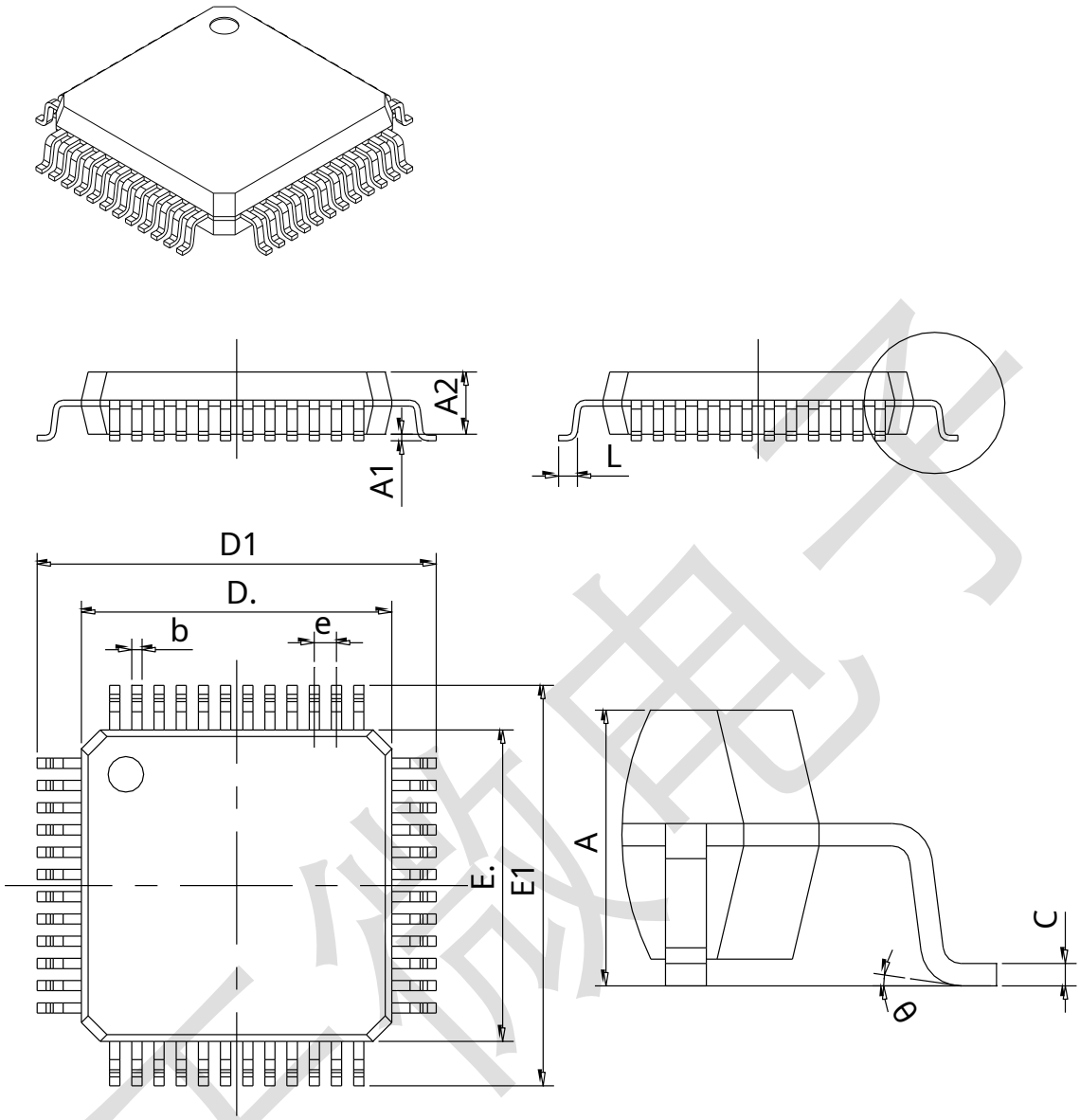
Command overview table:

command name	command code	D/C	Functional description	default
WRITE	1110-01A1A0	D.	write slave address	
Data Address (I2C)	0 A6 A5 A4 A3 A2 A1 A0	D.	write RAM address	
Data Format(I2C)	$D_{.A3}D_{.A2}D_{.A1}D_{.A0}D_{.B3}D_{.B2}D_{.B1}D_{.B0}$	D.	A3-A0 low four bits, B3-B0 high four bits	
SYS DIS	1000-0000	C	Turn off system clock and LED cycling	√
SYS EN	1000-0001	C	Turn on the system oscillator	
LED OFF	1000-0010	C	Turn off LED cycle	√
LED ON	1000-0011	C	Turn on the LED cycle	
BLINK OFF	1000-1000	C	turn off blinking	√
BLINK 2Hz	1000-1001	C	The LED flashes at a frequency of 2Hz	
BLINK_1Hz	1000-1010	C	The LED flashes at a frequency of 1Hz	
BLINK_0.5Hz	1000-1011	C	The LED flashes at a frequency of 0.5Hz	
SLAVE MODE	1001-0XXX	C	External oscillator, the clock is input from the OSC pin, The synchronization signal is input by the SYN pin	
RC Master Mode0	1001-100X	C	Built-in oscillator, OSC keeps low level, synchronous signal held high on the SYN pin should only for single chip	√
RC Master Mode1	1001-101X	C	Built-in oscillator, the internal frequency is output by OSC, The synchronization signal is output on the SYN pin	
EXT CLK Master Mode0	1001-110X	C	External oscillator, the clock is input from the OSC pin, The synchronization signal is held high by the SYN pin, Only referenced to single chip	√
EXT CLK Master Mode1	1001-111X	C	External oscillator, the clock is input from the OSC pin, The synchronization signal is output by the SYN pin	
COM Option	1010-abXX	C	When ab=00, 8COM Nmos; When ab=01, 16COM Nmos; When ab=10, 8COM Pmos; When ab=11, 16COM Pmos;	00
PWM Duty	1011-abcd	C	The change of abcd from 0-F corresponds to the 16-level brightness adjustment of 1/16--16/16 LEDs Festival	f

Note:

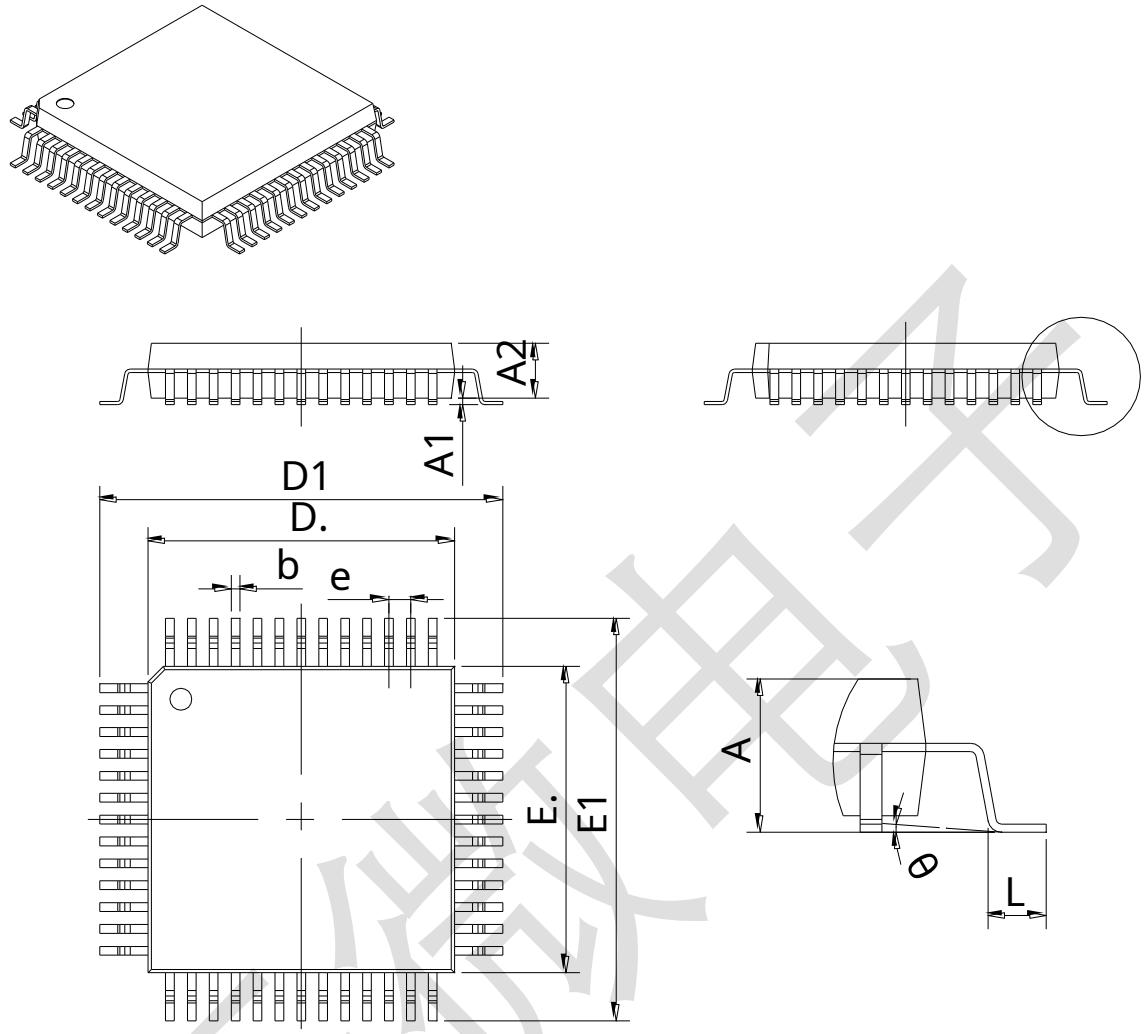
1. X does not care, it is recommended to write "0".
2. A6~A0 memory address.
3. D0~D3 memory data.
4. D/C data/command mode.
5. Default: the state of the chip after power-on reset

Package schematic diagram (LQFP48 7mm*7mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.500	0.053	0.059
b	0.180	0.270	0.007	0.010
c	0.130	0.180	0.005	0.007
D.	6.900	7.100	0.272	0.280
D1	8.800	9.200	0.346	0.362
E.	6.900	7.100	0.272	0.280
E1	8.800	9.200	0.346	0.362
e	0.500(BSC)		0.020(BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

Package schematic diagram (QFP52 14mm*14mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	- - -	1.600	- - -	0.063
A1	0.100		0.004	
A2	1.3500	1.500	0.053	0.059
b	0.400 (BSC)		0.016 (BSC)	
D.	13.900	14.100	0.547	0.555
D1	15.800	16.200	0.622	0.638
E.	13.900	14.100	0.547	0.555
E1	15.800	16.200	0.622	0.638
e	1.000 (BSC)		0.039(BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

All specs and applications shown above subject to change without prior notice.

(The above circuits and specifications are for reference only, if the company makes changes, we will not notify you in advance)