ES8311

Low Power Mono Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 100 dB signal to noise ratio, -93 dB THD+N
- One pair of analog input with differential input option
- Low noise pre-amplifier
- Noise reduction filters
- Auto level control (ALC) and noise gate
- Support analog and digital microphone

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 110 dB signal to noise ratio, -80 dB THD+N
- One pair of analog output with headphone driver and differential output option
- Dynamic range compression
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- 14 mW playback and record
- Low standby current

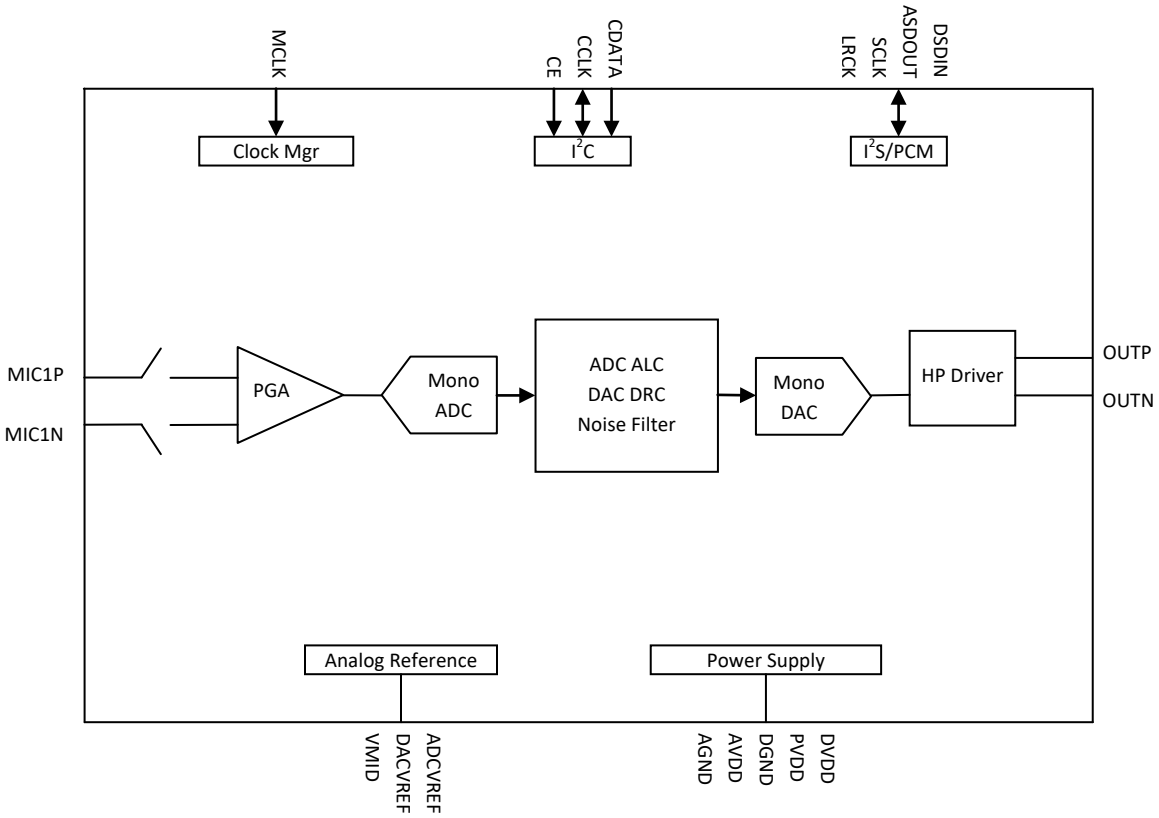
APPLICATIONS

- Automotive
- Phone
- Toy
- 2-way radio
- Dash cam
- IP Camera
- DVR, NVR
- Surveillance

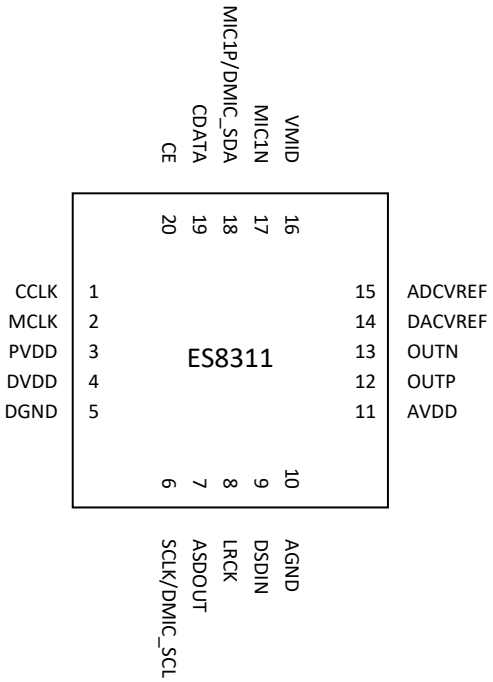
ORDERING INFORMATION

ES8311 -40°C ~ +105°C
QFN-20

1. BLOCK DIAGRAM

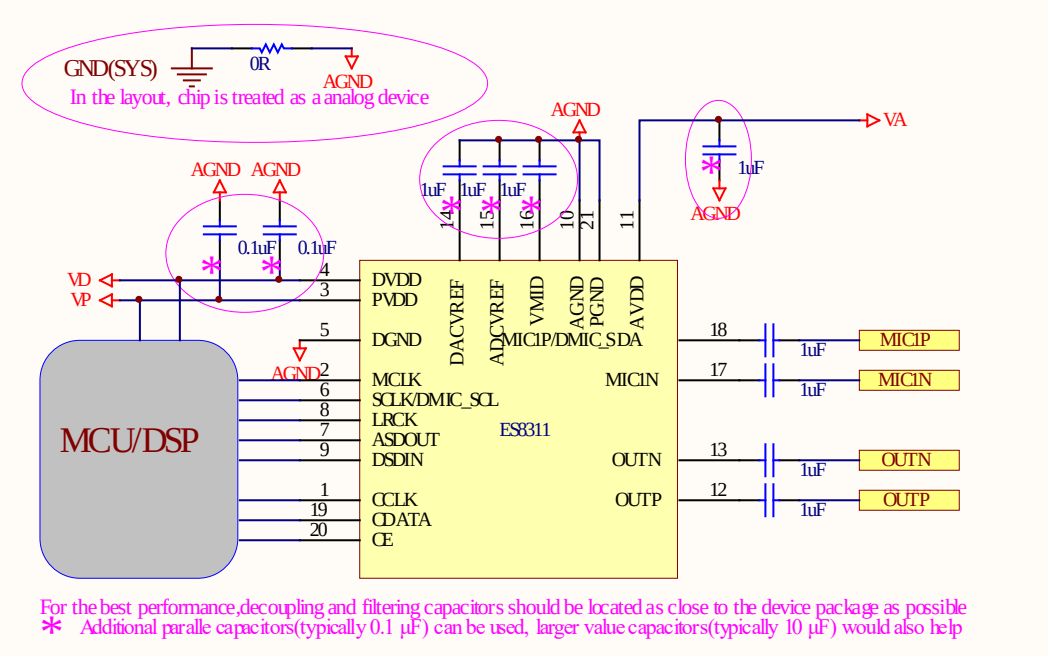


2. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA, CE	1, 19, 20	I, I/O, I	I^2C clock, data, address
MCLK	2	I	Master clock
SCLK/DMIC_SCL	6	I/O	Serial data bit clock/DMIC bit clock
LRCK	8	I/O	Serial data left and right channel frame clock
ASDOUT	7	O	ADC serial data output
DSDIN	9	I	DAC serial data input
MIC1P/DMIC_SDA MIC1N	18 17	I	Mic input
OUTP, OUTN	12, 13	O	Differential analog output
PVDD	3	Analog	Power supply for the digital input and output
DVDD, DGND	4, 5	Analog	Digital power supply
AVDD, AGND	11, 10	Analog	Analog power supply
VMID	16	Analog	Filtering capacitor connection
ADCVREF, DACVREF	15, 14	Analog	Filtering capacitor connection

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (64F, 128Fs, 256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (16 MHz, 25 MHz, 26 MHz, etc).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0011 00x, where x equals CE. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0011 00 CE	0	ACK	RAM	ACK	DATA	ACK	Stop

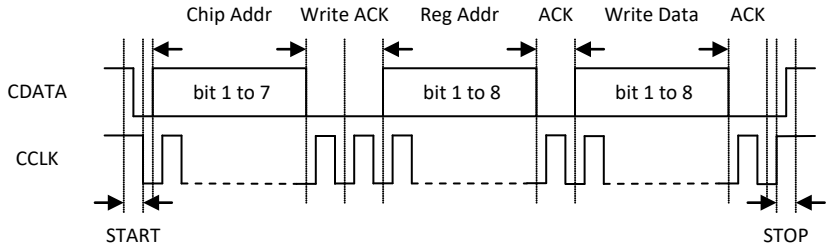


Figure 1a I^{2}C Write Timing

Table 2 Read Data from Register in I^{2}C Interface Mode

	Chip Address	R/W		Register Address		
Start	0011 00 CE	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0011 00 CE	1	ACK	Data	NACK	Stop

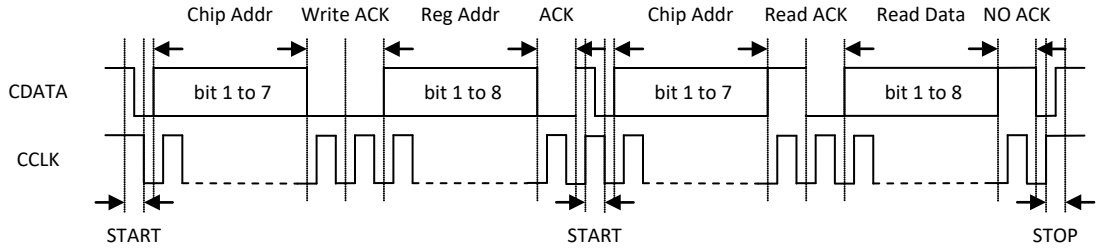


Figure 1b I^{2}C Read Timing

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and DSDIN or ASDOUT pins. These formats are I^2S, left justified, right justified and DSP/PCM. DAC input DSDIN is sampled by the device on the rising edge of SCLK. ADC data is out at ASDOUT on the falling edge of SCLK. The relationship of SDATA (DSIN/ASDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2d.

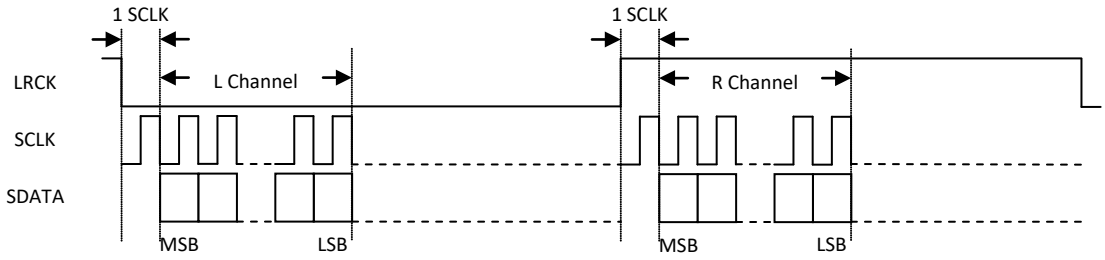


Figure 2a I^2S Serial Audio Data Format

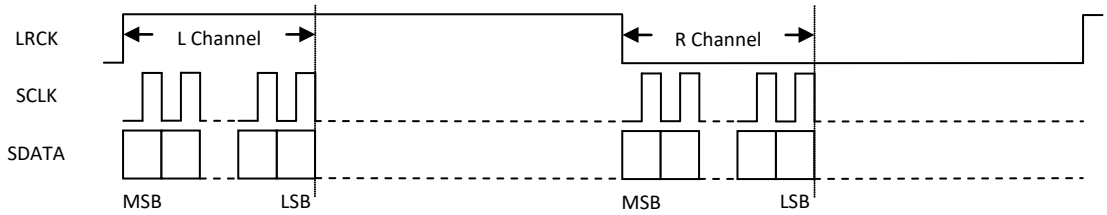


Figure 2b Left Justified Serial Audio Data Format

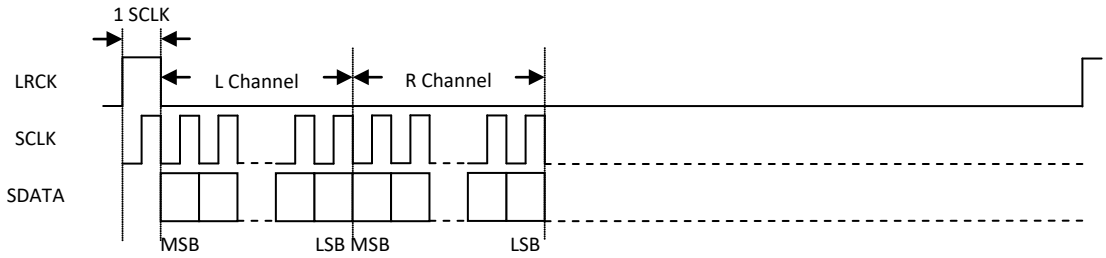


Figure 2c DSP/PCM Mode A Serial Audio Data Format

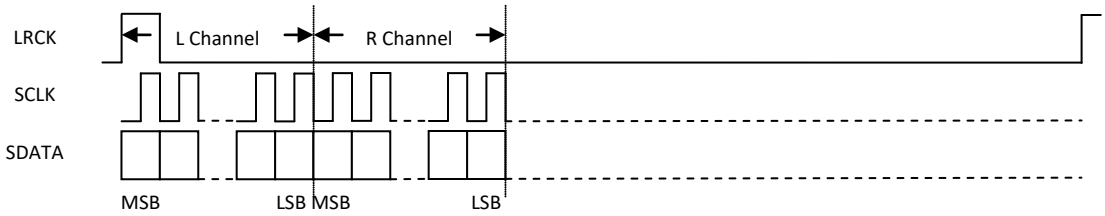


Figure 2d DSP/PCM Mode B Serial Audio Data Format

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+105°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
DVDD	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V
AVDD	1.7	1.8/3.3	3.6	V

Note 1: When REGISTER 0x02 MULT_PRE selection 2 or 3 is used, mclk_prediv must > 500 kHz when DVDD is 1.8V (±10%), or mclk_prediv must > 1 MHz when DVDD is 3.3V (±10%).

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	95	100	102	dB
THD+N	-95	-93	-85	dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level		±AVDD/3.3		Vrms
Input Impedance		6		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	105	110	115	dB
THD+N	-85	-80	-75	dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	56			dB
Analog Output				
Full Scale Output Level		±0.9*AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V		8		mA
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle (Note 2)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V	T_{SDO}		16	ns

	VDDD=1.8V			39	
LRCK edge to SDOUT valid (Note 3)	VDDD=3.3V VDDD=1.8V	T_{LDO}		11 25	ns
SDIN valid to SCLK rising setup time		T_{SDIS}	10		ns
SCLK rising to SDIN hold time		T_{SDIH}	10		ns

Note 2: one SCLK period of high time in DSP/PCM modes.

Note 3: only apply to MSB of Left Justified or DSP/PCM mode B.

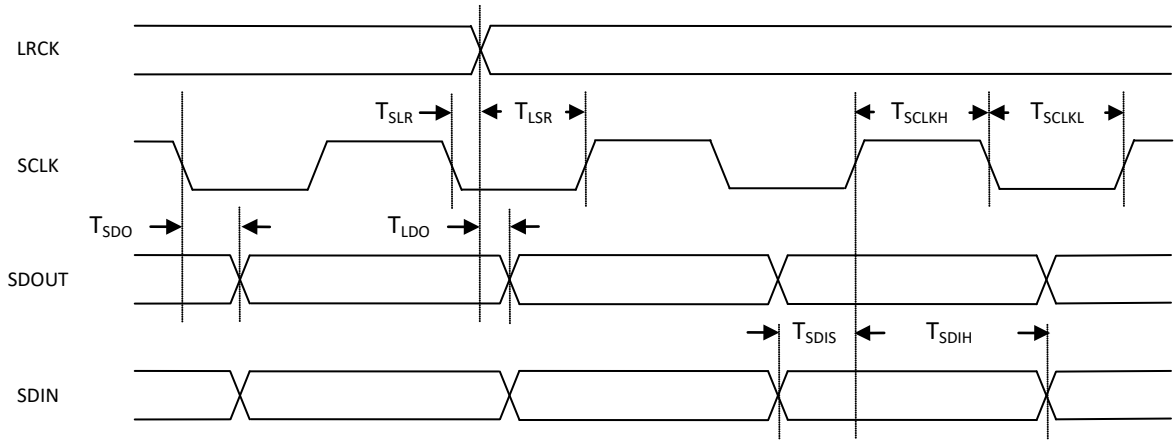


Figure 3 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

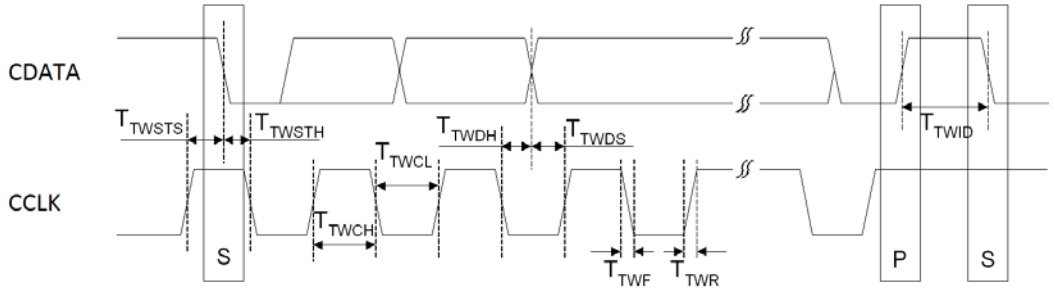


Figure 4 I²C Timing

8. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 –RESET, DEFAULT 0001 1111

Bit Name	Bit	Description
CSM_ON	7	Chip current state machine control 0 – csm power down (default) 1 – csm power on
MSC	6	0 – slave serial port mode (default) 1 – master serial port mode
SEQ_DIS	5	Power up sequence control 0 – power up sequence enable (default) 1 – power up sequence disabled
RST_DIG	4	Digital reset 0 – not reset 1 – reset digital except control port block (default)
RST_CMG	3	Clock manager block reset 0 – not reset 1 – reset clock manager block (default)
RST_MST	2	Master block reset 0 – not reset 1 – reset master block (default)
RST_ADC_DIG	1	ADC digital block reset 0 – not reset 1 – reset ADC digital block (default)
RST_DAC_DIG	0	DAC digital block reset 0 – not reset 1 – reset DAC digital block (default)

REGISTER 0X01 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
MCLK_SEL	7	Main clock (mclkin) select 0 – from MCLK (default) 1 – from BCLK
MCLK_INV	6	Main clock (mclkin) invert control 0 – normal MCLK (default) 1 – MCLK invert
MCLK_ON	5	MCLK in control 0 – MCLK off (default) 1 – MCLK on
BCLK_ON	4	SDP bit clock control 0 – BCLK off (default) 1 – BCLK on
CLKADC_ON	3	ADC digital clock control 0 – clk_adc off (default) 1 – clk_adc on
CLKDAC_ON	2	DAC digital clock control 0 – clk_dac off (default) 1 – clk_dac on
ANACLKADC_ON	1	ADC analog clock control 0 – anaclk_adc off

		1 – anaclk_adc on (default)
ANACLKDAC_ON	0	DAC analog clock control 0 – anaclk dac off 1 – anaclk_dac on (default)

REGISTER 0X02 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_PRE	7:5	Pre-divide mclkin control mclk_prediv=mclkin/(DIV_PRE+1)
MULT_PRE	4:3	Pre-multiply mclk_prediv 0 – dig_mclk=mclk_prediv*1 (default) 1 – dig_mclk=mclk_prediv*2 2 – dig_mclk=mclk_prediv*4 3 – dig_mclk=mclk_prediv*8
PATHSEL	2	Clock doubler path select 0 – no DFF path (default) 1 – DFF path
DELYSEL	1:0	clock doubler delay cell select 0 – 5ns (default) 1 – 10ns 2 – 15ns 3 – 15ns

REGISTER 0X03 – CLOCK MANAGER, DEFAULT 0001 0000

Bit Name	Bit	Description
ADC_FSMODE	6	adc fs mode 0 – single speed (default) 1 – double speed
ADC_OSR	5:0	ADC delta sigma over sample rate 0~14 – not use 15 – 60*fs(ss) / (ds not support) 16 – 64*fs(ss) / 32*fs(ds) (default) ... 31 – 124*fs(ss) / 62*fs(ds) 32 – 128*fs(ss) / 64*fs(ds) ... 63 – 252*fs(ss) / 126*fs(ds)

REGISTER 0X04 – CLOCK MANAGER, DEFAULT 0001 0000

Bit Name	Bit	Description
DAC_OSR	6:0	DAC over sample rate 0~14 – not use 15 – 60*fs (EQ not available) 16 – 64*fs (default) 17 – 68*fs ... 32 – 128*fs 64 – 256*fs ... 127 – 508*fs

REGISTER 0X05 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_CLKADC	7:4	adc_mclk clock divider adc_mclk=dig_mclk/(DIV_CLKADC+1)
DIV_CLKDAC	3:0	dac_mclk clock divider dac_mclk=dig_mclk/(DIV_CLKDAC+1)

REGISTER 0X06 – CLOCK MANAGER, DEFAULT 0000 0011

Bit Name	Bit	Description
BCLK_CON	6	BCLK out control when master mode 0 – normal continual BCLK out (default) 1 – stop BCLK out when data transfer finished
BCLK_INV	5	BCLK invert 0 – normal (default) 1 – BCLK invert
DIV_BCLK	4:0	BCLK divider at master mode 0~19 – MCLK/(DIV_BCLK+1) (default 3) 20 –MCLK /22 21 –MCLK /24 22 –MCLK /25 23 –MCLK /30 24 –MCLK /32 25 –MCLK /33 26 –MCLK /34 27 –MCLK /36 28 –MCLK /44 29 –MCLK /48 30 –MCLK /66 31 –MCLK /72 Note: “MCLK” here is “MCLK pin” when MCLK_SEL=0, is “BCLK pin” when MCLK_SEL=1 (refer to reg0x01[7])

REGISTER 0X07 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
TRI_BLRCK	5	BCLK/LRCK tri-state control 0 – normal (default) 1 – BCLK and LRCK tri-state output
TRI_ADCDAT	4	ADCDAT tri-state control 0 – normal (default) 1 – ADCDAT tri-state output
DIV_LRCK[11:8]	3:0	Master LRCK divider bit 11 to bit 8 LRCK (master)=MCLK/(LRCK_DIV+1) Note: “MCLK” here is “MCLK pin” when MCLK_SEL=0, is “BCLK pin” when MCLK_SEL=1 (refer to reg0x01[7])

REGISTER 0X08 – CLOCK MANAGER, DEFAULT 1111 1111

Bit Name	Bit	Description
DIV_LRCK[7:0]	7:0	Master LRCK divider bit 7 to bit 0 LRCK (master)=MCLK/(LRCK_DIV+1) DIV_LRCK=0 LRCK logic high level

		Note: “MCLK” here is “MCLK pin” when MCLK_SEL=0, is “BCLK pin” when MCLK_SEL=1 (refer to reg0x01[7])

REGISTER 0X09 – SDP, DEFAULT 0000 0000

Bit Name	Bit	Description
SDP_IN_SEL	7	SDP in data select 0 – Left channel data to DAC (default) 1 – right channel data to DAC
SDP_IN_MUTE	6	SDP in mute 0 – unmute (default) 1 – mute
SDP_IN_LRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity (default) 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after LRCK rising edge(default) 1 – MSB is available on 1st BCLK rising edge after LRCK rising edge
SDP_IN_WL	4:2	0 – 24-bit serial audio data word length (default) 1 – 20-bit serial audio data word length 2 – 18-bit serial audio data word length 3 – 16-bit serial audio data word length 4 – 32-bit serial audio data word length
SDP_IN_FMT	1:0	0 – I2S serial audio data format (default) 1 – left justify serial audio data format 2 – reserve 3 – DSP/PCM mode serial audio data format

REGISTER 0X0A – SDP, DEFAULT 0000 0000

Bit Name	Bit	Description
SDP_OUT_MUTE	6	SDP out mute 0 – unmute (default) 1 – mute
SDP_ OUT_LRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity (default) 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after LRCK rising edge (default) 1 – MSB is available on 1st BCLK rising edge after LRCK rising edge
SDP_OUT_WL	4:2	0 – 24-bit serial audio data word length (default) 1 – 20-bit serial audio data word length 2 – 18-bit serial audio data word length 3 – 16-bit serial audio data word length 4 – 32-bit serial audio data word length
SDP_OUT_FMT	1:0	0 – I2S serial audio data format (default) 1 – left justify serial audio data format 2 – reserve 3 – DSP/PCM mode serial audio data format

REGISTER 0X0B – SYSTEM, DEFAULT 0000 0000

Bit Name	Bit	Description
PWRUP_A	7:3	Power up stage A

		0~31：21us~232ms （LRCK=48KHz） 0~31：23us~253ms （LRCK=44.1KHz） 0~31：120us~1392ms （LRCK=8KHz）
PWRUP_B[3:1]	2:0	Power up stage B 0~31：21us~104ms （LRCK=48KHz） 0~31：23us~113ms （LRCK=44.1KHz） 0~31：120us~624ms （LRCK=8KHz）

REGISTER 0X0C – SYSTEM, DEFAULT 0010 0000

Bit Name	Bit	Description
PWRUP_B[0]	7	Power up stage B 0~31：21us~104ms （LRCK=48KHz） 0~31：23us~113ms （LRCK=44.1KHz） 0~31：120us~624ms （LRCK=8KHz）
PWRUP_C	6:0	Power up stage C 0~31：21us~234ms （LRCK=48KHz） 0~31：23us~254ms （LRCK=44.1KHz） 0~31：120us~1401ms （LRCK=8KHz）

REGISTER 0X0D – SYSTEM, DEFAULT 1111 1100

Bit Name	Bit	Description
PDN_ANA	7	0 – enable analog circuits 1 – power down analog circuits (default)
PDN_IBIASGEN	6	0 – enable analog bias circuits 1 – power down analog bias circuits (default)
PDN_ADCBIASGEN	5	0 – enable analog ADC bias circuits 1 – power down analog ADC bias circuits (default)
PDN_ADCVERFGEN	4	0 – enable analog ADC reference circuits 1 – power down analog ADC reference circuits (default)
PDN_DACVREFGEN	3	0 – enable analog DAC reference circuits 1 – power down analog DAC reference circuits (default)
PDN_VREF	2	0 – disable internal reference circuits 1 – enable reference circuits (default)
VMIDSEL	1:0	0 – vmid power down (default) 1 – start up vmid normal speed charge 2 – normal vmid operation 3 – start up vmid fast speed charge

REGISTER 0X0E – SYSTEM, DEFAULT 0110 1010

Bit Name	Bit	Description
PDN_PGA	6	0 – enable analog PGA 1 – power down analog PGA (default)
PDN_MOD	5	0 – enable analog ADC modulator 1 – power down analog ADC modulator (default)
RST_MOD	4	0 – disable (default) 1 – reset modulator
VROI	3	0 – normal impedance 1 – low impedance (default)
LPVREFBUF	2	0 – normal mode of internal reference voltage (default) 1 – low power mode of internal reference voltage

REGISTER 0X0F – SYSTEM, DEFAULT 0000 0000

Bit Name	Bit	Description
LPDAC	7	0 – normal mode (default) 1 – low power mode for DAC
LPPGA	6	0 – normal mode (default) 1 – low power mode for PGA
LPPGAOUT	5	0 – normal mode (default) 1 – low power mode for PGA output
LPVCMMOD	4	0 – normal mode (default) 1 – low power mode for ADC
LPADCVRP	3	0 – normal mode (default) 1 – low power mode for ADC reference
LPDACVRP	2	0 – normal mode (default) 1 – low power mode for DAC reference
LPFLASH	1	0 – normal mode (default) 1 – low power mode for ADC
LPINT1	0	0 – normal mode (default) 1 – low power mode for ADC

REGISTER 0X10 – SYSTEM, DEFAULT 0001 0011

Bit Name	Bit	Description
SYNCMODE	7	0 – normal (default) 1 – sync mode
VMIDLOW	6:5	0 – vmid='vdda/2' (default) 1 – vmid='vdda/2-75mv' 2 – vmid='vdda/2-145mv' 3 – vmid='vdda/2-175mv'
DAC_IBIAS_SW	4	0 – normal DAC bias setting 1 – higher DAC bias setting (default)
IBIAS_SW	3:2	0 –bias setting level0 (default) 1 –bias setting level1 2 –bias setting level2 3 –bias setting level3 (highest bias)
VX2OFF	1	0 – enable internal reference voltage doubler 1 – off (default)
VX1SEL	0	0 – vx1=1.45v 1 – vx1=1.65v (default)

REGISTER 0X11 – SYSTEM, DEFAULT 0111 1100

Bit Name	Bit	Description
VSEL	6:0	Internal use

REGISTER 0X12 – SYSTEM, DEFAULT 0000 0010

Bit Name	Bit	Description
PDN_DAC	1	0 – enable DAC 1 – power down DAC (default)
ENREFR	0	0 – disable internal reference circuits for DAC output (default) 1 – enable reference circuits for DAC output

REGISTER 0X13 – SYSTEM, DEFAULT 0100 0000

Bit Name	Bit	Description
HPSW	4	0 – default for line out drive (default) 1 – enable output to HP drive

REGISTER 0X14 – SYSTEM, DEFAULT 0001 0000

Bit Name	Bit	Description
DMIC_ON	6	DMIC SDA selection 0 – no DMIC 1 – select DMIC and DMIC_SDA from MIC1P
LINSEL	4	0 – no input selection 1 – select Mic1p-Mic1n
PGAGAIN	3:0	ADC PGA gain 0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB

REGISTER 0X15 – ADC, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_RAMPRATE	7:4	ADC VC ramp rate 0 – disable soft ramp 1 – 0.25dB/4LRCK 2 – 0.25dB/8LRCK 3 – 0.25dB/16LRCK 4 – 0.25dB/32LRCK 5 – 0.25dB/64LRCK 6 – 0.25dB/128LRCK 7 – 0.25dB/256LRCK 8 – 0.25dB/512LRCK 9 – 0.25dB/1024LRCK 10 – 0.25dB/2048LRCK 11 – 0.25dB/4096LRCK 12 – 0.25dB/8192LRCK 13 – 0.25dB/16384LRCK 14 – 0.25dB/32768LRCK 15 – 0.25dB/65536LRCK
DMIC_SENSE	0	DMIC data latch sense 0 – at clock positive edge 1 – at clock negative edge

REGISTER 0X16 – ADC, DEFAULT 0000 0100

Bit Name	Bit	Description

ADC_SYNC	5	synchronize filter counter with LRCK 0 – non standard audio clock 1 – standard audio clock
ADC_INV	4	ADC polarity inverted 0 – normal 1 – inverted
ADC_ RAMCLR	3	adc ram clear when lrck/adc_mclk active
ADC_ SCALE	2:0	ADC gain scale up 0 – 0dB 1 – 6dB 2 – 12dB 3 – 18dB 4 – 24dB (default) 5 – 30dB 6 – 36dB 7 – 42dB

REGISTER 0X17 – ADC, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_VOLUME	7:0	ADC volume 0x00 – -95.5dB (default) 0x01 – -90.5dB ⋯ 0.5dB/step 0xBE – -0.5dB 0xBF – 0dB 0xC0 – +0.5dB ⋯ 0xFF – +32dB When ALC is on, ADC_VOLUME = MAXGAIN

REGISTER 0X18 – ADC, DEFAULT 0000 0000

Bit Name	Bit	Description
ALC_EN	7	ADC auto level control enable 0 – ALC disable (default) 1 – ALC enable
ADC_AUTOMUTE_EN	6	ADC automute enable 0 – automute disable (default) 1 – automute enable
ALC_WINSIZE	3:0	winsize for alc 0 – 0.25dB/2LRCK 1 – 0.25dB/4LRCK ... 15 – 0.25dB/65536LRCK

REGISTER 0X19 – ADC, DEFAULT 0000 0000

Bit Name	Bit	Description
ALC_MAXLEVEL	7:4	ALC target max level 0 – -30.1dB 1 – -24.1dB 2 – -20.6dB 3 – -18.1dB

		4 – -16.1dB 5 – -14.5dB 6 – -13.2dB 7 – -12.0dB 8 – -11.0dB 9 – -10.1dB 10 – -9.3 dB 11 – -8.5 dB 12 – -7.8 dB 13 – -7.2 dB 14 – -6.6 dB 15 – -6.0 dB
ALC_MINLEVEL	3:0	ALC target min level 0 – -30.1dB 1 – -24.1dB 2 – -20.6dB 3 – -18.1dB 4 – -16.1dB 5 – -14.5dB 6 – -13.2dB 7 – -12.0dB 8 – -11.0dB 9 – -10.1dB 10 – -9.3 dB 11 – -8.5 dB 12 – -7.8 dB 13 – -7.2 dB 14 – -6.6 dB 15 – -6.0 dB

REGISTER 0X1A – ADC, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_AUTOMUTE_WS	7:4	ADC automute winsize Detect samples= (2^11)*(winsize+1) 0 – 2048 samples - 42ms 1 – 4096 samples - 84ms ... 15 – 32768 samples - 688ms
ADC_AUTOMUTE_NG	3:0	ADC automute noise gate 0 – -96dB 1 – -90dB 2 – -84dB 3 – -78dB 4 – -72dB 5 – -66dB 6 – -60dB 7 – -54dB 8 – -51dB 9 – -48dB 10 – -45dB 11 – -42dB 12 – -39dB

		13 – -36dB 14 – -33dB 15 – -30dB

REGISTER 0X1B – ADC, DEFAULT 0000 1100

Bit Name	Bit	Description
ADC_AUTOMUTE_VOL	7:5	ADC auto mute out gain select out gain=ADC_AUTOMUTE_VOL * -4dB 0 – mute to 0dB ⋯ -4dB/step 7 – mute to -28dB
ADC_HPFS1	4:0	ADCHPF stage1 coeff

REGISTER 0X1C – ADC, DEFAULT 0100 1100

Bit Name	Bit	Description
ADC_EQBYPASS	6	ADCEQ bypass 0 – normal 1 – bypass (default)
ADC_HPF	5	ADC offset freeze 0 – freeze offset 1 – dynamic HPF
ADC_HPFS2	4:0	ADCHPF stage2 coeff

REGISTER 0X1D – ADC, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B0[29:24]	5:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X1E – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B0[23:16]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X1F – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B0[15:8]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X20 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B0[7:0]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X21 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A1[29:24]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X22 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A1[23:16]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X23 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A1[15:8]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X24 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A1[7:0]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X25 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A2[29:24]	7:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X26 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A2[23:16]	7:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X27 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A2[15:8]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X28 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_A2[7:0]	7:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X29 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B1[29:24]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X2A – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B1[23:16]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X2B – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B1[15:8]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X2C – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B1[7:0]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X2D – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B2[29:24]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X2E – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description

ADCEQ_B2[23:16]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X2F – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B2[15:8]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X30 – ADCEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCEQ_B2[7:0]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X31 – DAC, DEFAULT 0000 0000

Bit Name	Bit	Description
DAC_DSMMUTE_TO	7	DAC DSM mute target 0 – mute to 8 (default) 1 – mute to 7/9
DAC_DSMMUTE	6	DAC DSM mute control 0 – unmute (default) 1 – mute
DAC_DEMMUTE	5	DAC DEM mute control 0 – unmute (default) 1 – mute
DAC_INV	4	DAC data inversion control 0 – data no phase inversion (default) 1 – data 180 degree phase inversion
DAC_RAMCLR	3	DAC ram clear when lrck/dac_mclk active 0 – normal (default) 1 – clear RAM
DAC_DSMDITH_OFF	2	DAC DSM dither control 0 – dither on (default) 1 – dither off

REGISTER 0X32 – DAC, DEFAULT 0000 0000

Bit Name	Bit	Description
DAC_VOLUME	7:0	DAC volume 0x00 – -95.5dB (default) 0x01 – -95.0dB ⋯ 0.5dB/step 0xBE – -0.5dB 0xBF – 0dB 0xC0 – +0.5dB ⋯ 0xFF – +32dB When DRC is on, ADC_VOLUME = MAXGAIN

REGISTER 0X33 – DAC, DEFAULT 0000 0000

Bit Name	Bit	Description
DAC_OFFSET	7:0	DAC offset

REGISTER 0X34 – DAC, DEFAULT 0000 0000

Bit Name	Bit	Description
DRC_EN	7	DAC data range control enable 0 – disable DRC (default) 1 – enable DRC
DRC_WINSIZE	3:0	winsize for DRC cnt_timer [DRC_WINSIZE] 0 – 0.25dB/2LRCK (default) 1 – 0.25dB/4LRCK ... 15 – 0.25dB/65536LRCK

REGISTER 0X35 – DAC, DEFAULT 0000 0000

Bit Name	Bit	Description
DRC_MAXLEVEL	7:4	DRC target max level 0 – -30.1dB (default) 1 – -24.1dB 2 – -20.6dB 3 – -18.1dB 4 – -16.1dB 5 – -14.5dB 6 – -13.2dB 7 – -12.0dB 8 – -11.0dB 9 – -10.1dB 10 – -9.3 dB 11 – -8.5 dB 12 – -7.8 dB 13 – -7.2 dB 14 – -6.6 dB 15 – -6.0 dB
DRC_MINLEVEL	3:0	DRC target min level 0 – -30.1dB (default) 1 – -24.1dB 2 – -20.6dB 3 – -18.1dB 4 – -16.1dB 5 – -14.5dB 6 – -13.2dB 7 – -12.0dB 8 – -11.0dB 9 – -10.1dB 10 – -9.3 dB 11 – -8.5 dB 12 – -7.8 dB 13 – -7.2 dB 14 – -6.6 dB 15 – -6.0 dB

REGISTER 0X36 – DAC, DEFAULT 0000 0000

Bit Name	Bit	Description

REGISTER 0X37 – DAC, DEFAULT 0000 1000

Bit Name	Bit	Description
DAC_RAMPRATE	7:4	DAC VC/DRC ramp rate 0 – disable soft ramp (default) 1 – 0.25dB/4LRCK 2 – 0.25dB/8LRCK 3 – 0.25dB/16LRCK 4 – 0.25dB/32LRCK 5 – 0.25dB/64LRCK 6 – 0.25dB/128LRCK 7 – 0.25dB/256LRCK 8 – 0.25dB/512LRCK 9 – 0.25dB/1024LRCK 10 – 0.25dB/2048LRCK 11 – 0.25dB/4096LRCK 12 – 0.25dB/8192LRCK 13 – 0.25dB/16384LRCK 14 – 0.25dB/32768LRCK 15 – 0.25dB/65536LRCK
DAC_EQBYPASS	3	DACEQ bypass 0 – enable (default) 1 – bypass

REGISTER 0X38 – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B0[29:24]	5:0	30-bit B0 coefficient for DACEQ

REGISTER 0X39 – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B0[23:16]	7:0	30-bit B0 coefficient for DACEQ

REGISTER 0X3A – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B0[15:8]	7:0	30-bit B0 coefficient for DACEQ

REGISTER 0X3B – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B0[7:0]	7:0	30-bit B0 coefficient for DACEQ

REGISTER 0X3C – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B1[29:24]	7:0	30-bit B1 coefficient for DACEQ

REGISTER 0X3D – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B1[23:16]	7:0	30-bit B1 coefficient for DACEQ

REGISTER 0X3E – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B1[15:8]	7:0	30-bit B1 coefficient for DACEQ

REGISTER 0X3F – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_B1[7:0]	7:0	30-bit B1 coefficient for DACEQ

REGISTER 0X40 – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_A1[29:24]	7:0	30-bit A1 coefficient for DACEQ

REGISTER 0X41 – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_A1[23:16]	7:0	30-bit A1 coefficient for DACEQ

REGISTER 0X42 – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_A1[15:8]	7:0	30-bit A1 coefficient for DACEQ

REGISTER 0X43 – DACEQ, DEFAULT 0000 0000

Bit Name	Bit	Description
DACEQ_A1[7:0]	7:0	30-bit A1 coefficient for DACEQ

REGISTER 0X44 – GPIO, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC2DAC_SEL	7	ADC data to DAC 0 – disable (default) 1 – ADC to DAC
ADCDAT_SEL	6:4	ADCDAT output select 0 – ADC + ADC (default) 1 – ADC + 0 2 – 0 + ADC 3 – 0 + 0 4 – DACL + ADC 5 – ADC + DACR 6 – DACL + DACR 7 – NA
I2C_WL	3	Internal use
GPIO_SEL	2:0	Internal use

REGISTER 0X45 – GP, DEFAULT 0000 0000

Bit Name	Bit	Description
FORCECSM	7:4	Internal use
ADC_DLY_SEL	3	Internal use
DAC_DLY_SEL	2	Internal use
DAC_AUTOCHN	1	Internal use
PULLUP_SE	0	BCLK/LRCK pullup control

		0 – pullup on (default) 1 – pullup off

REGISTER 0XFA – I2C, DEFAULT 0000 0000

Bit Name	Bit	Description
I2C_RETIME	1	Internal use
INI_REG	0	Initial registers 0 – not reset (default) 1 – reset registers to default except itself

REGISTER 0XFC – FLAG, DEFAULT 0000 0000

Bit Name	Bit	Description
FLAG_CSM_CHIP	6:4	Chip state machine, read only 0 – S0 1 – S1 2 – S2 3 – S3 6 – S6 7 – S7 other: dummy state
FLAG_ADCAM	1	ADC automute flag, read only
FLAG_DACAM	0	Internal use

REGISTER 0XFD – CHIP, DEFAULT 1000 0011

Bit Name	Bit	Description
CHIP_ID1	7:0	Chip ID information, 0x83

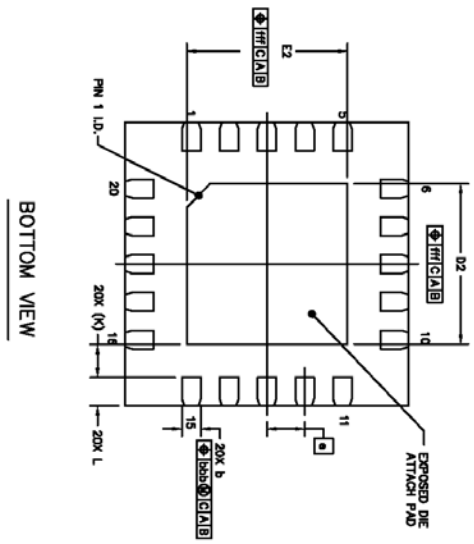
REGISTER 0XFE – CHIP, DEFAULT 0001 0001

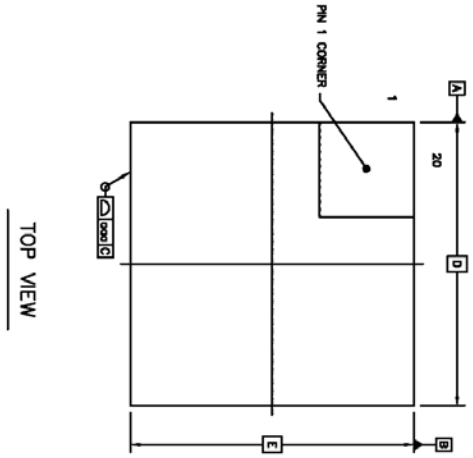
Bit Name	Bit	Description
CHIP_ID2	7:0	Chip ID information, 0x11

REGISTER 0XFF – CHIP, DEFAULT 0000 0000

Bit Name	Bit	Description
CHIP_VER	7:0	Chip version information, 0x00

9. PACKAGE (UNIT: MM)





	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	----	0.4	----
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		3 BSC	
BODY SIZE Y	E		3 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	1.6	1.7	1.8
EP SIZE Y	E2	1.6	1.7	1.8
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.35 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

10.CORPORATE INFORMATION

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